DS1922L, DS1922T

Temperature Logger iButton With 8kB Datalog Memory

www.maxim-ic.com

GENERAL DESCRIPTION

The DS1922L/T temperature logger iButtons® are rugged, self-sufficient systems that measure temperature and record the result in a protected memory section. The recording is done at a user-defined rate. A total of 8192 8-bit readings or 4096 16-bit readings taken at equidistant intervals ranging from 1s to 273hrs can be stored. In addition to this, there are 512 bytes of SRAM for storing application-specific information and 64 bytes for calibration data. A mission to collect data can be programmed to begin immediately, or after a user-defined delay or after a temperature alarm. Access to the memory and control functions can be password protected. The DS1922L/T is configured and communicates with a host computing device through the serial 1-Wire® protocol, which requires only a single data lead and a ground return. Every DS1922L/T is factory-lasered with a guaranteed unique 64-bit registration number that allows for absolute traceability. The durable stainless-steel package is highly resistant to environmental hazards such as dirt, moisture, and shock. Accessories permit the DS1922L/T to be mounted on almost any object, including containers, pallets, and bags.

APPLICATIONS

Temperature Logging in Cold Chain, Food Safety, Bio Science, and Pharmaceutical and Medical Products

High-Temperature Logging (Process Monitoring, Industrial Temperature Monitoring)

ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
DS1922L-F5	-40°C to +85°C	F5 iButton
DS1922T-F5	0°C to +125°C	F5 iButton

See page 11 for Common iButton Features and Examples of Accessories.

Commands, Registers, and Modes are capitalized for clarity.

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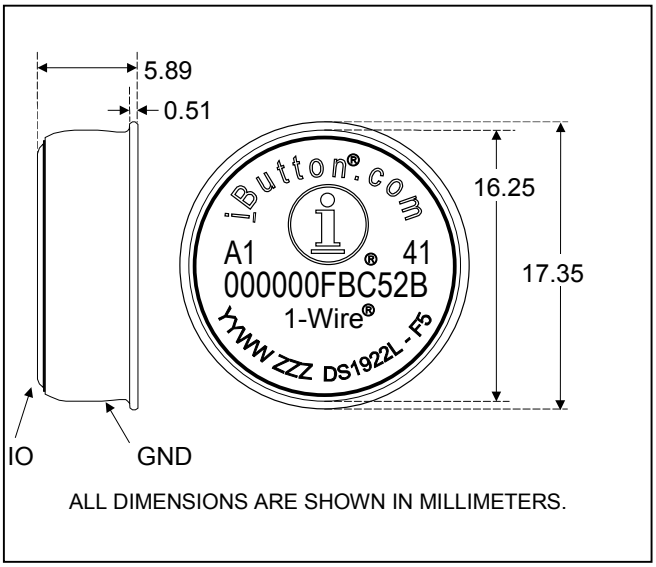
SPECIAL FEATURES

- Automatically Wakes up, Measures Temperature, and Stores Values in 8kB of Datalog Memory in 8- or 16-Bit Format
- Digital Thermometer Measures Temperature with 8-Bit (0.5°C) or 11-Bit (0.0625°C) Resolution
- Accuracy Better than ±0.5°C from -10°C to +65°C (DS1922L), ±0.5°C from +20°C to +75°C (DS1922T) with Software Correction
- Sampling Rate from 1s up to 273hrs
- Programmable Recording Start Delay After Elapsed Time or Upon a Temperature Alarm Trip Point
- Programmable High and Low Trip Points for Temperature Alarms
- Quick Access to Alarmed Devices Through 1-Wire Conditional Search Function
- 512 Bytes of General-Purpose Plus 64 Bytes of Calibration Memory
- Two-Level Password Protection of All Memory and Configuration Registers
- Communicates to Host with a Single Digital Signal at up to 15.4kbps at Standard Speed or up to 125kbps in Overdrive Mode Using 1-Wire Protocol
- Operating Range: DS1922L: -40 to +85°C; DS1922T: 0 to +125°C

PIN CONFIGURATION



ALL DIMENSIONS ARE SHOWN IN MILLIMETERS.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

ABSOLUTE MAXIMUM RATINGS

I/O Voltage to GND	-0.3V, +6V
I/O Sink Current	20mA
Operating Temperature Range (DS1922L)	-40°C to +85°C
Operating Temperature Range (DS1922T)	0°C to +125°C
Junction Temperature	+150°C
Storage Temperature Range (DS1922L)	-40°C to +85°C*
Storage Temperature Range (DS1922T)	0°C to +125°C*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to the absolute maximum rating conditions for extended periods may affect device.

**Storage or operation above +50°C significantly reduces battery life.*

ELECTRICAL CHARACTERISTICS

(V_{PUP} = 3.0V to 5.25V, T_A = -40°C to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O Pin General Data						
1-Wire Pullup Resistance	R_{PUP}	(Notes 1, 2)			2.2	kΩ
Input Capacitance	C_{IO}	(Note 3)		100	800	pF
Input Load Current	I_L	I/O pin at V_{PUP}		6	10	µA
High-to-Low Switching Threshold	V_{TL}	(Notes 4, 5)	0.4		3.2	V
Input Low Voltage	V_{IL}	(Notes 1, 6)			0.3	V
Low-to-High Switching Threshold	V_{TH}	(Notes 4, 7)	0.7		3.4	V
Switching Hysteresis	V_{HY}	(Note 8)	0.09		N/A	V
Output Low Voltage	V_{OL}	At 4mA (Note 9)			0.4	V
Recovery Time (Note 1)	t_{REC}	Standard speed, R_{PUP} = 2.2kΩ	5			µs
		Overdrive speed, R_{PUP} = 2.2kΩ	2			
		Overdrive speed, directly prior to reset pulse; R_{PUP} = 2.2kΩ	5			
Rising-Edge Hold-Off Time	t_{REH}	(Note 10)	0.6		2.0	µs
Timeslot Duration (Note 1)	t_{SLOT}	Standard speed	65			µs
		Overdrive speed, V_{PUP} > 4.5V	8			
		Overdrive speed (Note 11)	9.5			
I/O Pin, 1-Wire Reset, Presence Detect Cycle						
Reset Low Time (Note 1)	t_{RSTL}	Standard speed, V_{PUP} > 4.5V	480		720	µs
		Standard speed (Note 11)	690		720	
		Overdrive speed, V_{PUP} > 4.5V	48		80	
		Overdrive speed (Note 11)	70		80	
Presence Detect High Time	t_{PDH}	Standard speed, V_{PUP} > 4.5V	15		60	µs
		Standard speed (Note 11)	15		63.5	
		Overdrive speed (Note 11)	2		7	
Presence Detect Fall Time (Note 12)	t_{FPD}	Standard speed, V_{PUP} > 4.5V	1.5		5	µs
		Standard speed	1.5		8	
		Overdrive speed	0.15		1	
Presence Detect Low Time	t_{PDL}	Standard speed, V_{PUP} > 4.5V	60		240	µs
		Standard speed (Note 11)	60		287	
		Overdrive speed, V_{PUP} > 4.5V (Note 11)	7		24	
		Overdrive speed (Note 11)	7		28	
Presence Detect Sample Time (Note 1)	t_{MSP}	Standard speed, V_{PUP} > 4.5V	65		75	µs
		Standard speed	71.5		75	
		Overdrive speed	8		9	
I/O Pin, 1-Wire Write						
Write-0 Low Time (Note 1)	t_{W0L}	Standard speed	60		120	µs
		Overdrive Speed, V_{PUP} > 4.5V (Note 11)	6		12	
		Overdrive speed (Note 11)	7.5		12	
Write-1 Low Time (Notes 1, 13)	t_{W1L}	Standard speed	5		15 - ε	µs
		Overdrive speed	1		1.95 - ε	

I/O Pin, 1-Wire Read					
Read Low Time (Notes 1, 14)	t_{RL}	Standard speed	5	15 - δ	µs
		Overdrive speed	1	1.95 - δ	
Read Sample Time (Notes 1, 14)	t_{MSR}	Standard speed	t_{RL} + δ	15	µs
		Overdrive speed	t_{RL} + δ	1.95	
Real Time Clock					
Accuracy		+25°C	-2	+2	min/ month
Frequency Deviation	Δ_F	-40°C to +85°C	-300	+60	PPM
		0°C to +125°C	-600	+60	
Temperature Converter					
Conversion Time (Note 15)	t_{CONV}	8-bit mode	30	75	ms
		16-bit mode (11 bits)	240	600	
Thermal Response Time Constant (note 16)	τ_{RESP}	iButton package	130		s
Conv. Error Without Software Correction (note 17)	$\Delta\vartheta$		See Temperature Accuracy Graphs		°C
Conv. Error With Software Correction (Note 18)	$\Delta\vartheta$		See Temperature Accuracy Graphs		°C

Note 1: System Requirement
Note 2: Maximum allowable pullup resistance is a function of the number of 1-Wire devices in the system and 1-Wire recovery times. The specified value here applies to systems with only one device and with the minimum 1-Wire recovery times. For more heavily loaded systems, an active pullup such as that found in the DS2480B may be required.
Note 3: Capacitance on the data pin could be 800pF when V_{PUP} is first applied. If a 2.2kΩ resistor is used to pull up the data line, 2.5µs after V_{PUP} has been applied the parasite capacitance will not affect normal communications.
Note 4: V_{TL}, V_{TH} are a function of the internal supply voltage.
Note 5: Voltage below which, during a falling edge on I/O, a logic '0' is detected.
Note 6: The voltage on I/O needs to be less or equal to V_{ILMAX} whenever the master drives the line low.
Note 7: Voltage above which, during a rising edge on I/O, a logic '1' is detected.
Note 8: After V_{TH} is crossed during a rising edge on I/O, the voltage on I/O has to drop by V_{HY} to be detected as logic '0'.
Note 9: The I-V characteristic is linear for voltages less than 1V.
Note 10: The earliest recognition of a negative edge is possible at t_{REH} after V_{TH} has been previously reached.
Note 11: Highlighted numbers are NOT in compliance with the published iButton standards. See comparison table below.
Note 12: Interval during the negative edge on I/O at the beginning of a Presence Detect pulse between the time at which the voltage is 90% of V_{PUP} and the time at which the voltage is 10% of V_{PUP}.
Note 13: ε represents the time required for the pullup circuitry to pull the voltage on I/O up from V_{IL} to V_{TH}.
Note 14: δ represents the time required for the pullup circuitry to pull the voltage on I/O up from V_{IL} to the input high threshold of the bus master.
Note 15: To conserve battery power, use 8-bit temperature logging whenever possible.
Note 16: This number was derived from a test conducted by Cemagref in Antony, France, in July of 2000. http://www.cemagref.fr/English/index.htm Test Report No. E42.
Note 17: Includes ±0.15°C oven measurement uncertainty.
Note 18: Assumes using calibration memory with calibration equations for error compensation. Includes ±0.15°C oven measurement uncertainty. Guaranteed by design.

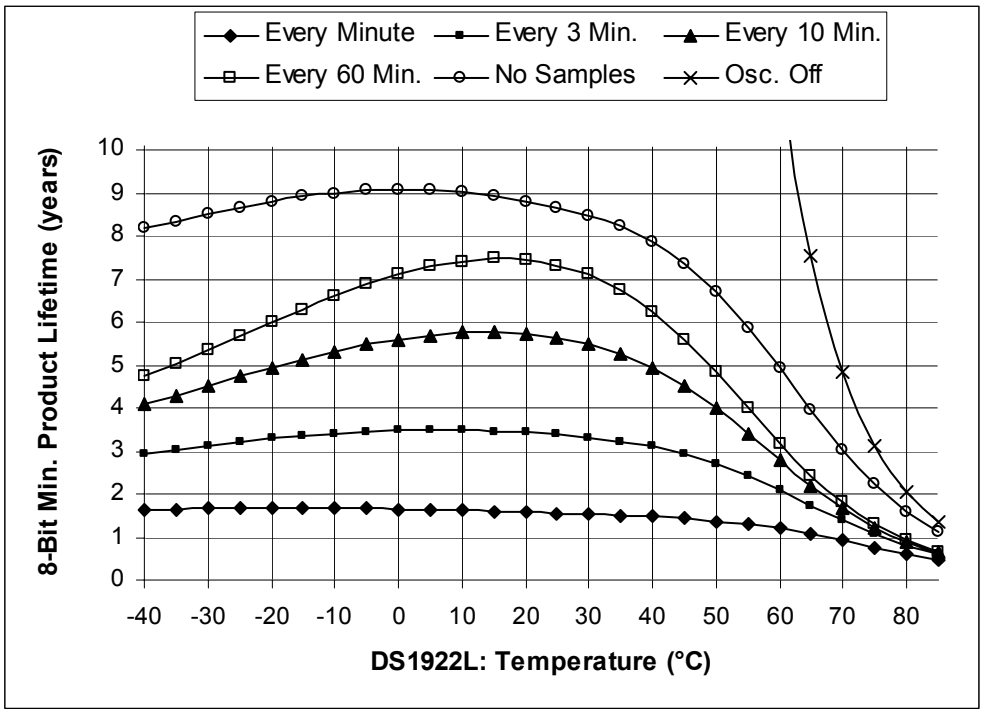
PARAMETER NAME	STANDARD VALUES				DS1922L/T VALUES			
	STANDARD SPEED		OVERDRIVE SPEED		STANDARD SPEED		OVERDRIVE SPEED	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
t_{SLOT} (incl. t_{REC})	61µs	(undef.)	7µs	(undef.)	65µs[1)]	(undef.)	9.5µs	(undef.)
t_{RSTL}	480µs	(undef.)	48µs	80µs	690µs	720µs	70µs	80µs
t_{PDH}	15µs	60µs	2µs	6µs	15µs	63.5µs	2µs	7µs
t_{PDL}	60µs	240µs	8µs	24µs	60µs	287µs	7µs	28µs
t_{W0L}	60µs	120µs	6µs	16µs	60µs	120µs	7.5µs	12µs

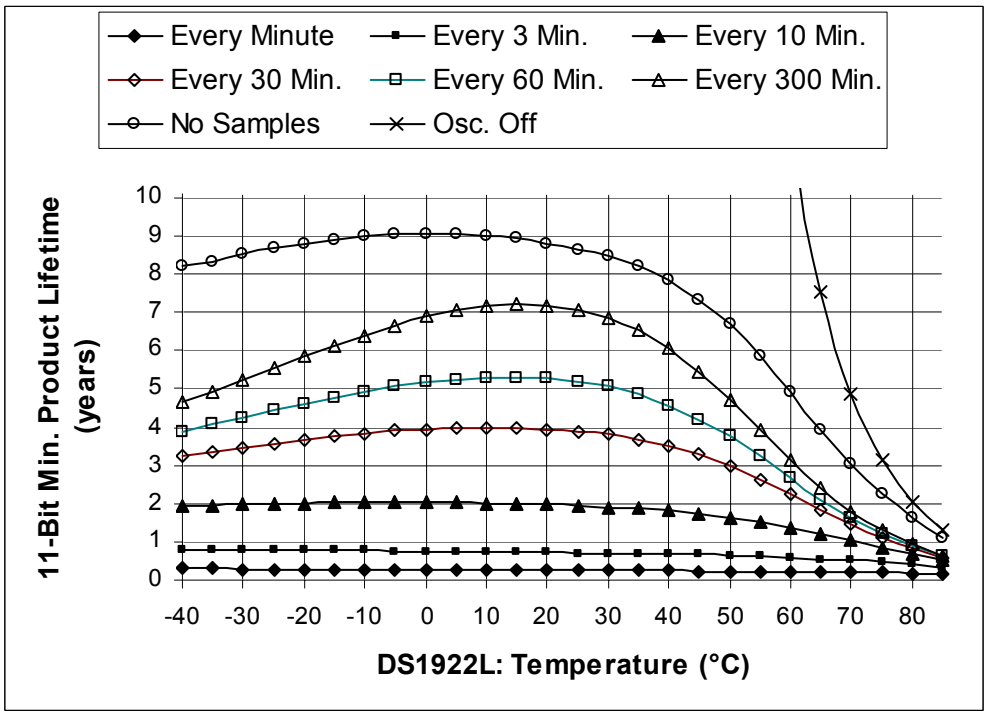
[1)] Intentional change, longer recovery time requirement due to modified 1-Wire front end.

PHYSICAL SPECIFICATION

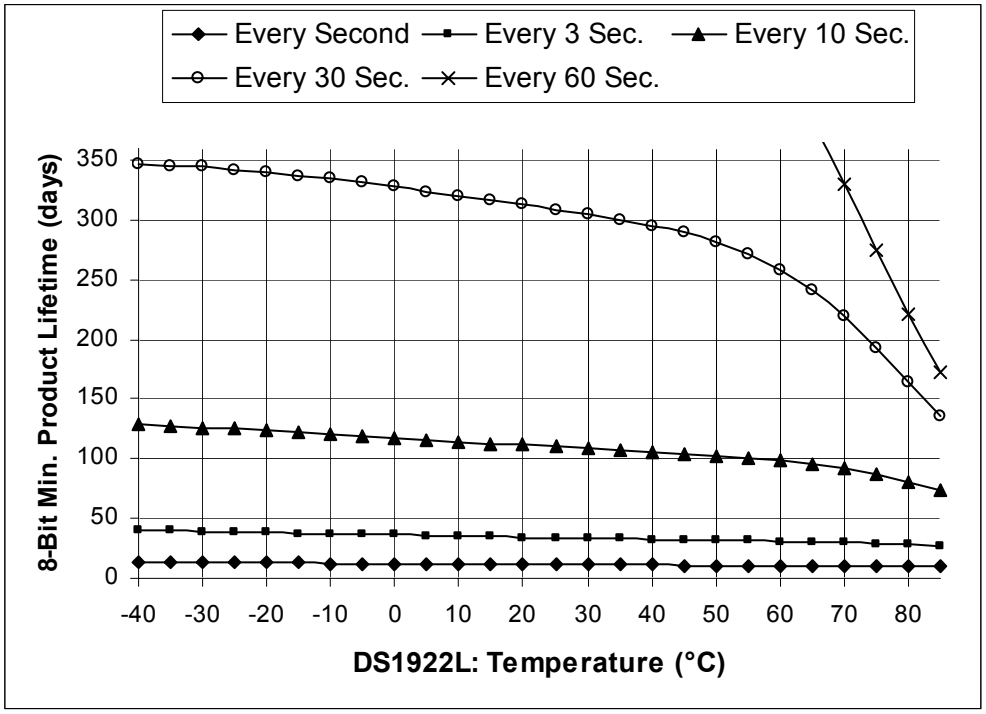
Size	See mechanical drawing
Weight	Ca. 3.3 grams
Safety	Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus, approval under Entity Concept for use in Class I, Division 1, Group A, B, C, and D Locations (application pending)

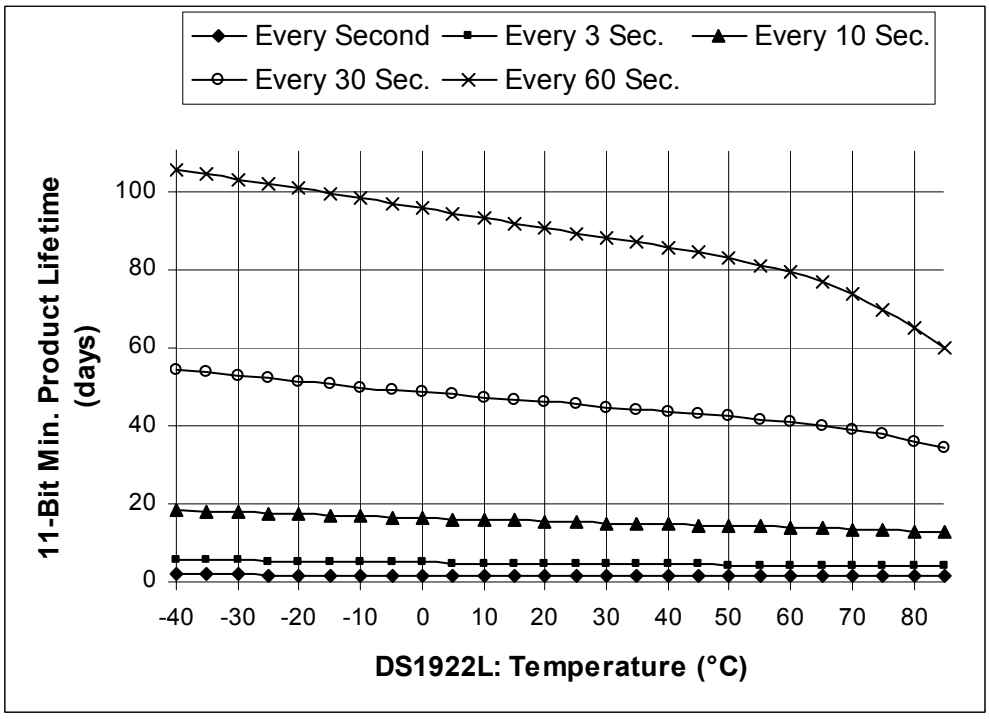
DS1922L MINIMUM PRODUCT LIFETIME VS. TEMPERATURE, SLOW SAMPLING



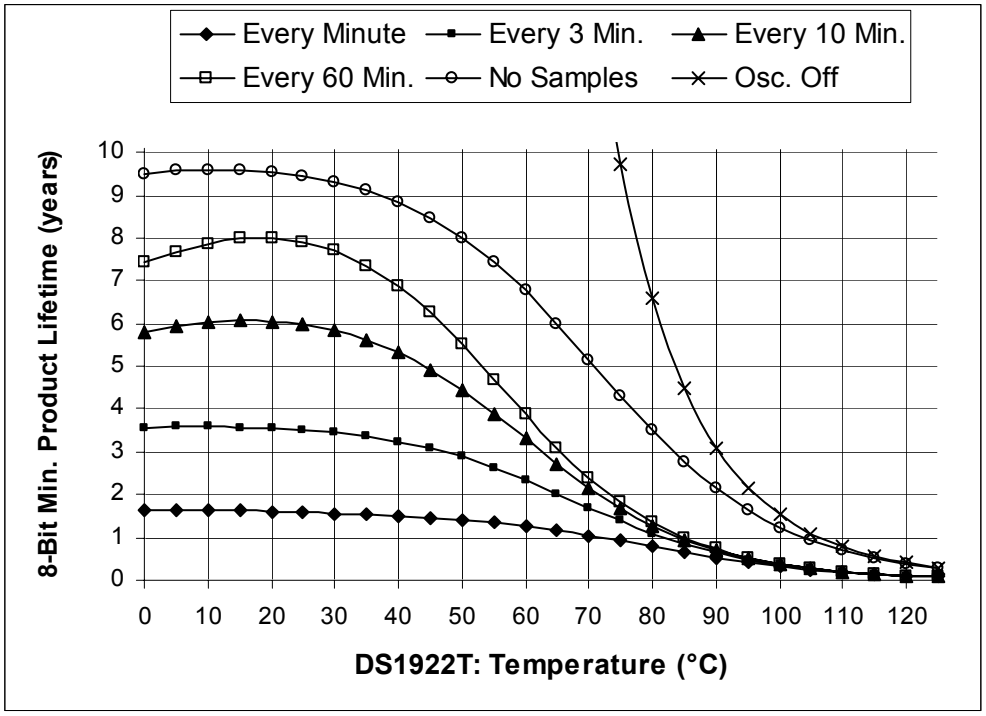


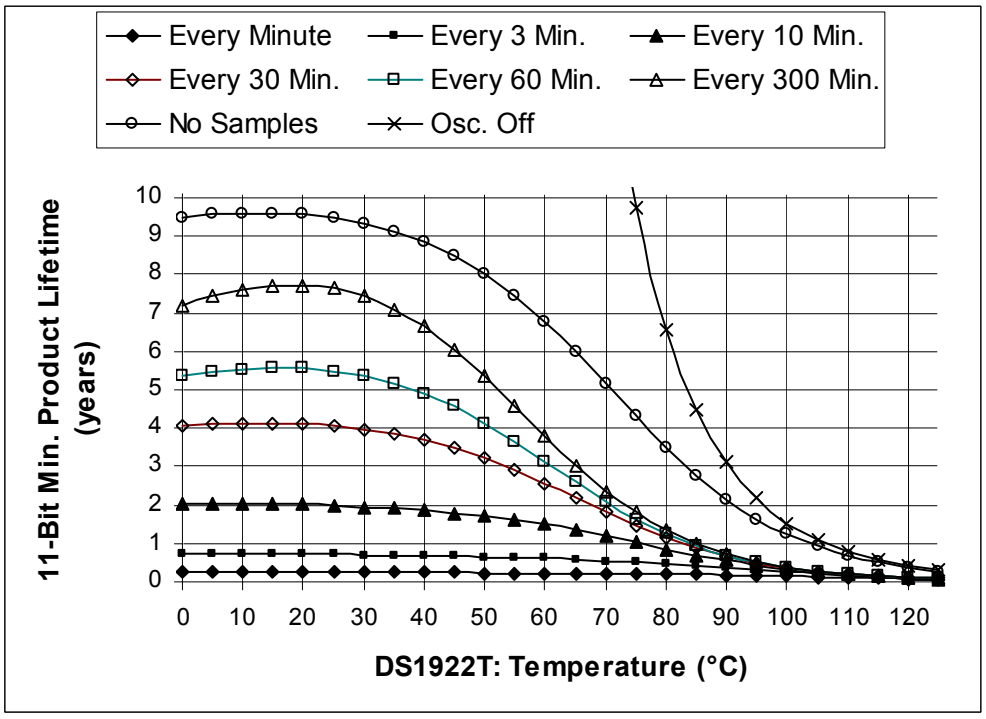
DS1922L MINIMUM PRODUCT LIFETIME VS. TEMPERATURE, FAST SAMPLING



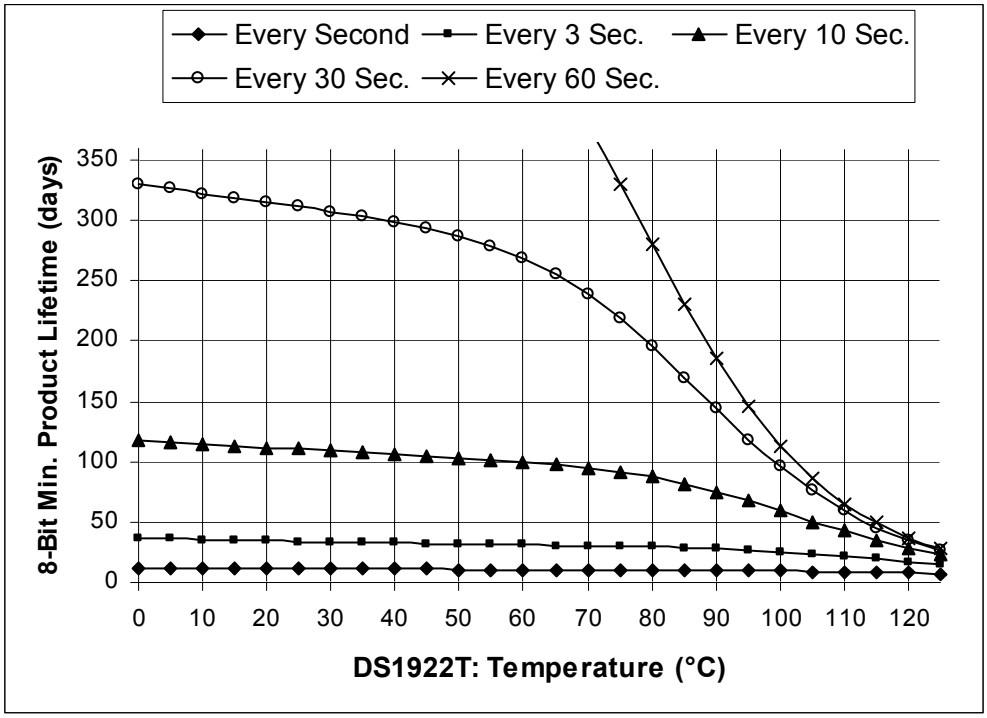


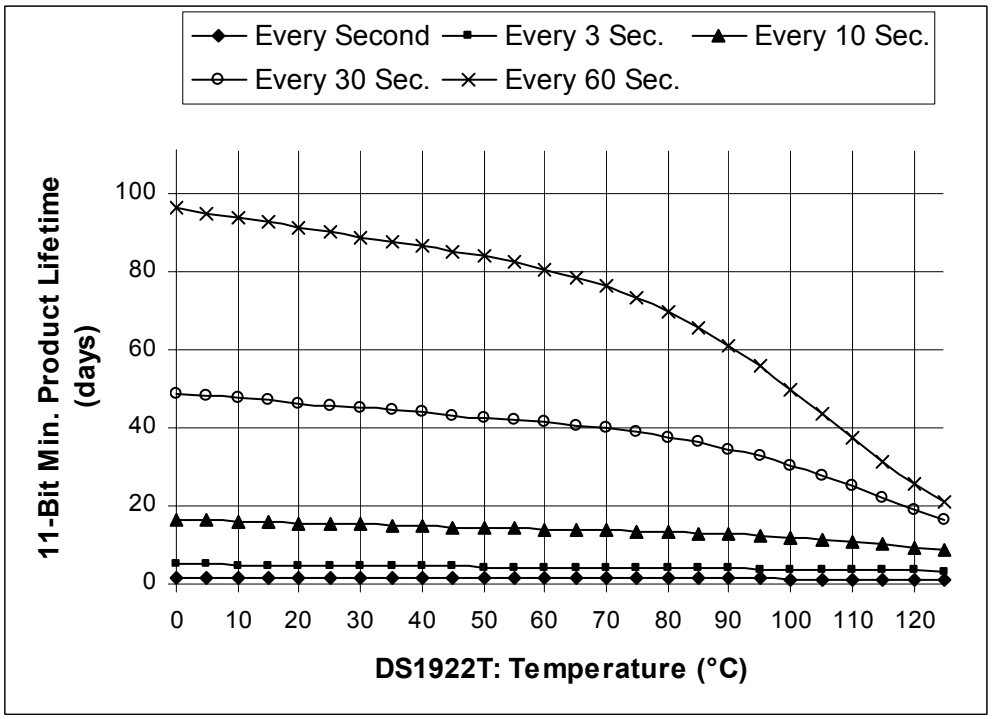
DS1922T MINIMUM PRODUCT LIFETIME VS. TEMPERATURE, SLOW SAMPLING



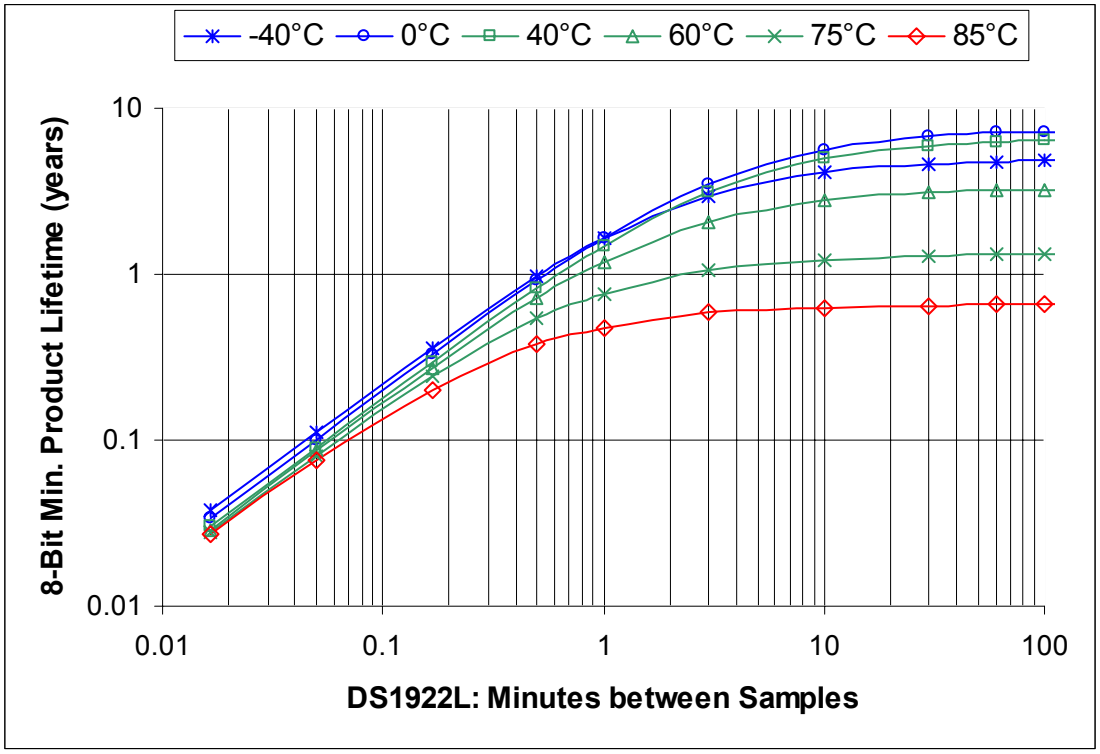


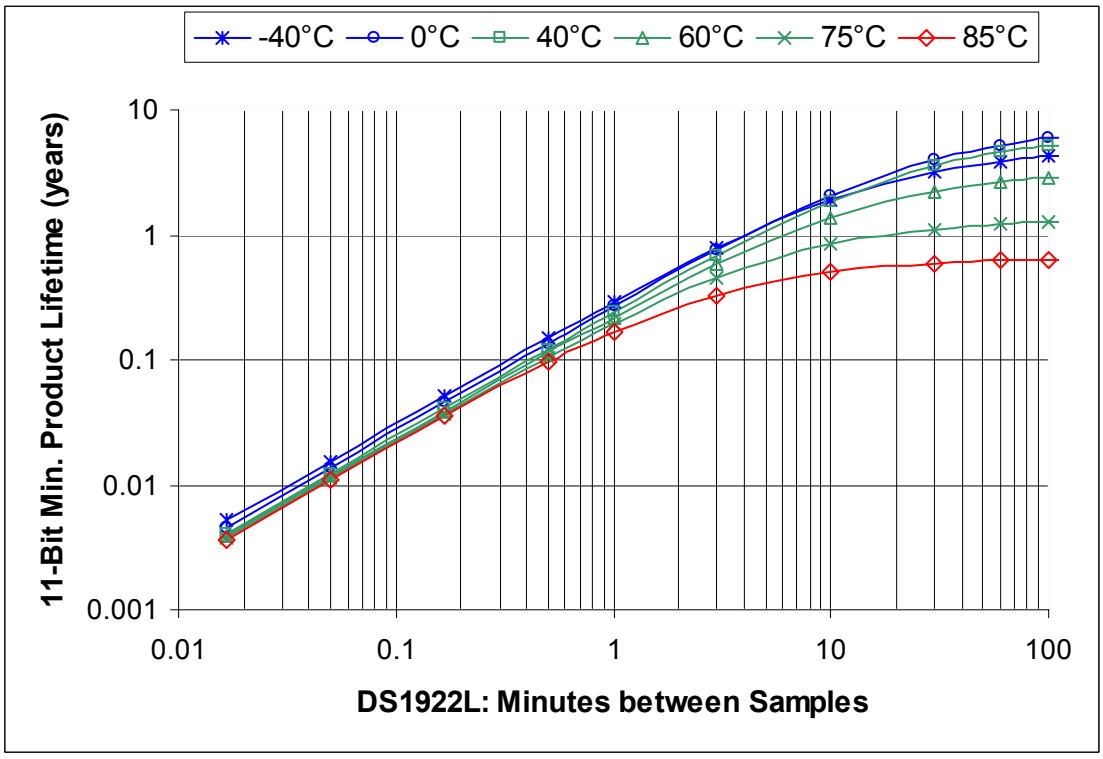
DS1922T MINIMUM PRODUCT LIFETIME VS. TEMPERATURE, FAST SAMPLING



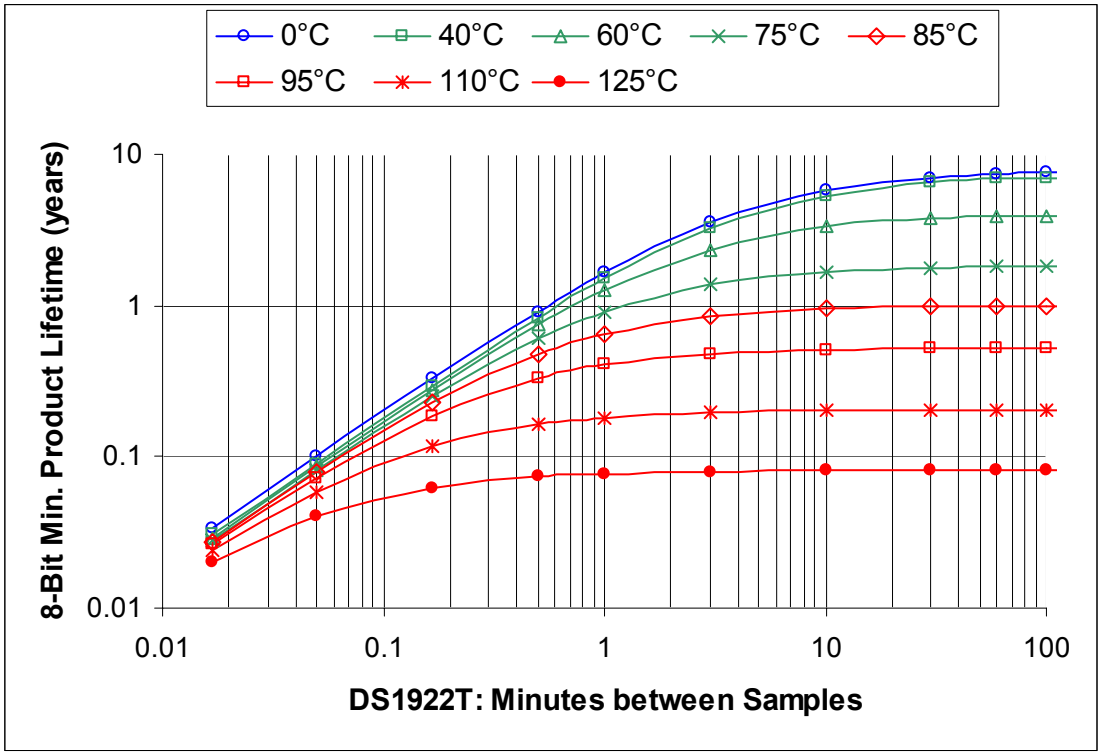


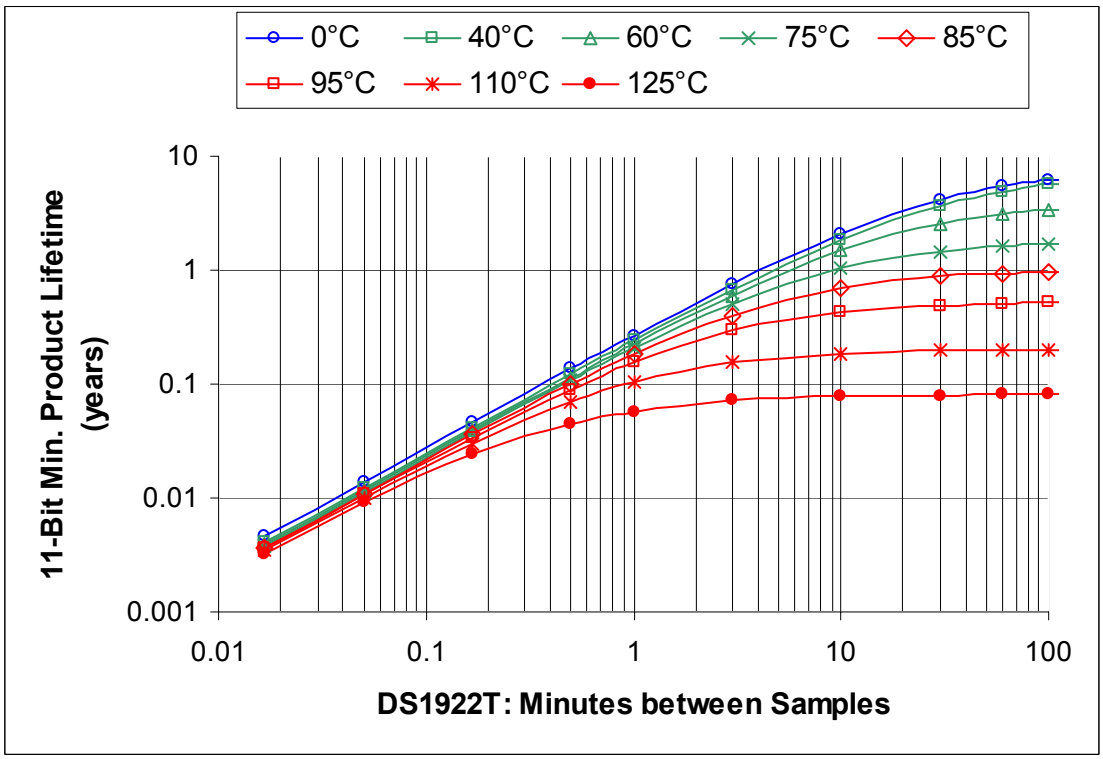
DS1922L MINIMUM PRODUCT LIFETIME VS. SAMPLE RATE



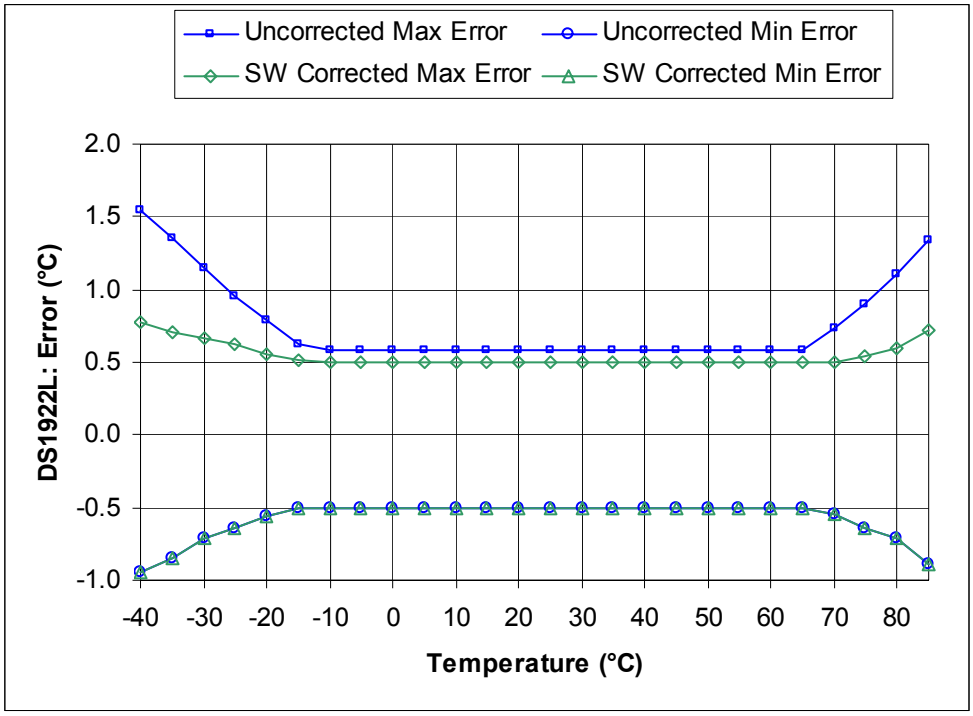


DS1922T MINIMUM PRODUCT LIFETIME VS. SAMPLE RATE



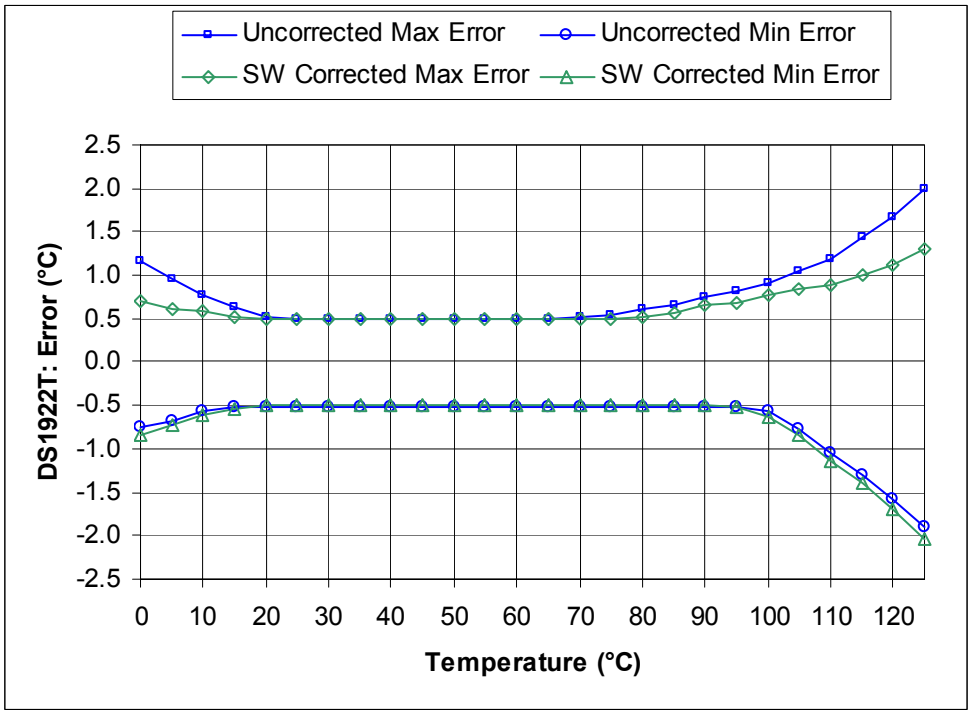


DS1922L TEMPERATURE ACCURACY



NOTE: The graphs are based on preliminary data.

DS1922T TEMPERATURE ACCURACY



NOTE: The graphs are based on preliminary data.

COMMON iButton FEATURES

- Digital identification and information by momentary contact.
- Unique factory-lasered 64-bit registration number assures error free device selection and absolute traceability because no two parts are alike.
- Built-in multidrop controller for 1-Wire net.
- Chip-based data carrier compactly stores information.
- Data can be accessed while affixed to object.
- Button shape is self-aligning with cup-shaped probes.
- Durable stainless-steel case engraved with registration number withstands harsh environments.
- Easily affixed with self-stick adhesive backing, latched by its flange, or locked with a ring pressed onto its rim.
- Presence detector acknowledges when reader first applies voltage.
- Meets UL#913 (4th Edit.); Intrinsically Safe Apparatus: approved under Entity Concept for use in Class I, Division 1, Group A, B, C, and D Locations (application pending).

EXAMPLES OF ACCESSORIES

DS9096P	Self-Stick Adhesive Pad
DS9101	Multipurpose Clip
DS9093RA	Mounting Lock Ring
DS9093A	Snap-In Fob
DS9092	iButton Probe

APPLICATION

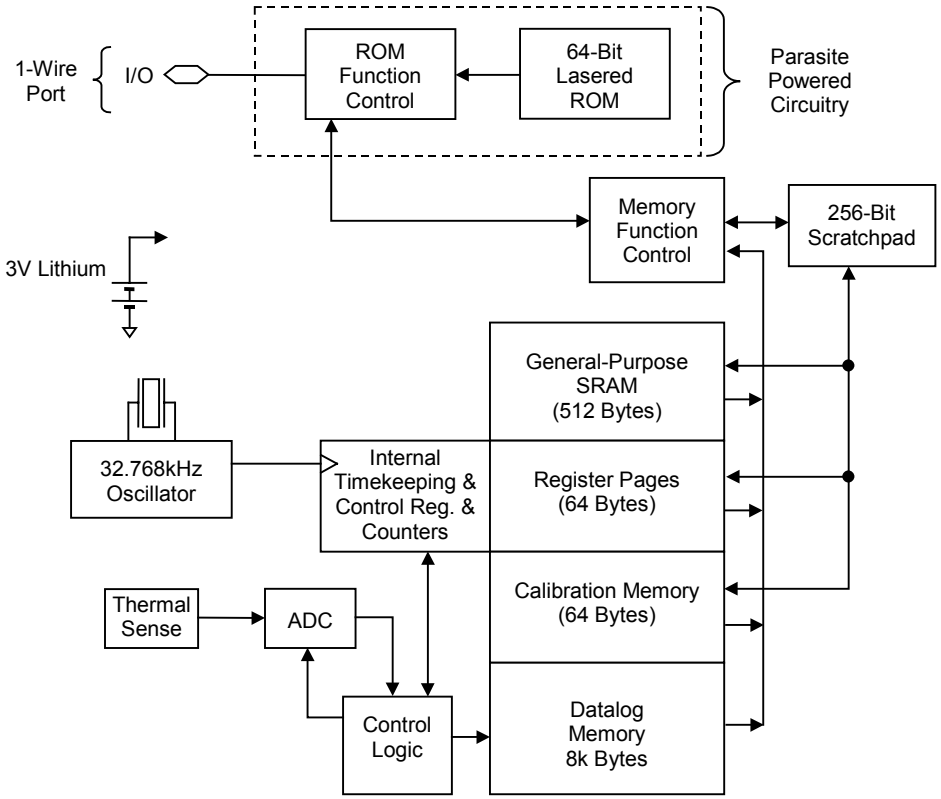
The DS1922L is an ideal device to monitor for extended periods of time the temperature of any object it is attached to or shipped with, such as fresh produce, medical drugs and supplies and for use in refrigerators and freezers. With its shifted temperature range, the DS1922T is suited to monitor processes that require temperatures close to the boiling point of water, such as pasteurization of food items. Software for setup and data retrieval through the 1-Wire interface is available for free download from the iButton website (www.ibutton.com). This software also includes drivers for the serial and USB port of a PC, and routines to access the general-purpose memory for storing application- or equipment-specific data files.

OVERVIEW

The block diagram in Figure 1 shows the relationships between the major control and memory sections of the DS1922L/T. The device has six main data components: 1) 64-bit lasered ROM, 2) 256-bit scratchpad, 3) 512-byte general-purpose SRAM, 4) two 256-bit register pages of timekeeping, control, status, and counter registers and passwords, 5) 64 bytes of calibration memory, and 6) 8192 bytes of data-logging memory. Except for the ROM and the scratchpad, all other memory is arranged in a single linear address space. The data-logging memory, counter registers, and several other registers are read-only for the user. Both register pages are write-protected while the device is programmed for a mission. The password registers, one for a read password and another one for a read/write password can only be written, never read.

Figure 1 shows the hierarchical structure of the 1-Wire protocol. The bus master must first provide one of the eight ROM function commands: 1) Read ROM, 2) Match ROM, 3) Search ROM, 4) Conditional Search ROM, 5) Skip ROM, 6) Overdrive-Skip ROM, 7) Overdrive-Match ROM or 8) Resume. Upon completion of an Overdrive ROM command byte executed at standard speed, the device will enter Overdrive mode, where all subsequent communication occurs at a higher speed. The protocol required for these ROM function commands is described in Figure 11. After a ROM function command is successfully executed, the memory and control functions become accessible and the master may provide any one of the nine available commands. The protocol for these memory and control function commands is described in Figure 9. **All data is read and written least significant bit first.**

Figure 1. DS1922L/T Block Diagram



PARASITE POWER

The block diagram (Figure 1) shows the parasite-powered circuitry. This circuitry "steals" power whenever the I/O input is high. I/O will provide sufficient power as long as the specified timing and voltage requirements are met. The advantages of parasite power are two-fold: 1) by parasiting off this input, battery power is conserved; and 2) if the battery is exhausted for any reason, the ROM may still be read.

64-BIT LASERED ROM

Each DS1922L/T contains a unique ROM code that is 64 bits long. The first 8 bits are a 1-Wire family code. The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits. See Figure 3 for details. The 1-Wire CRC is generated using a polynomial generator consisting of a shift register and XOR gates as shown in Figure 4. The polynomial is $X^8 + X^5 + X^4 + 1$. Additional information about the Dallas 1-Wire Cyclic Redundancy Check (CRC) is available *in Application Note 27* and in the *Book of DS19xx iButton Standards*.

The shift register bits are initialized to 0. Then starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8^{th} bit of the family code has been entered, then the serial number followed by the temperature range code is entered. After the range code has been entered, the shift register contains the CRC value. Shifting in the 8 bits of CRC returns the shift register to all 0s.

Figure 2. Hierachical Structure for 1-Wire Protocol

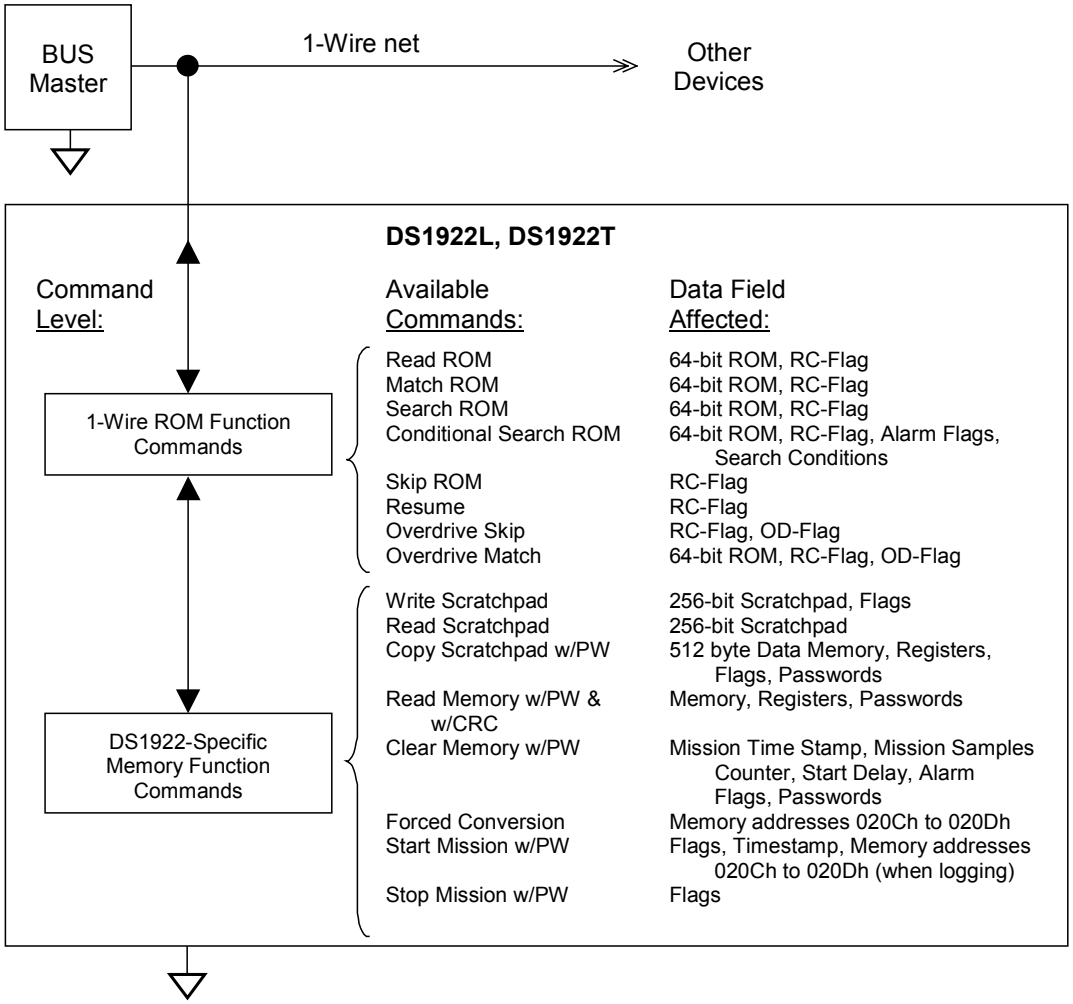


Figure 3. 64-Bit Lasered ROM

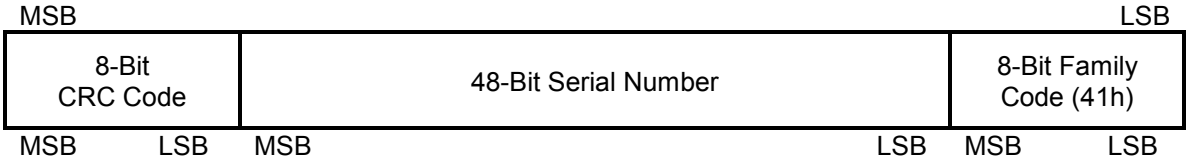
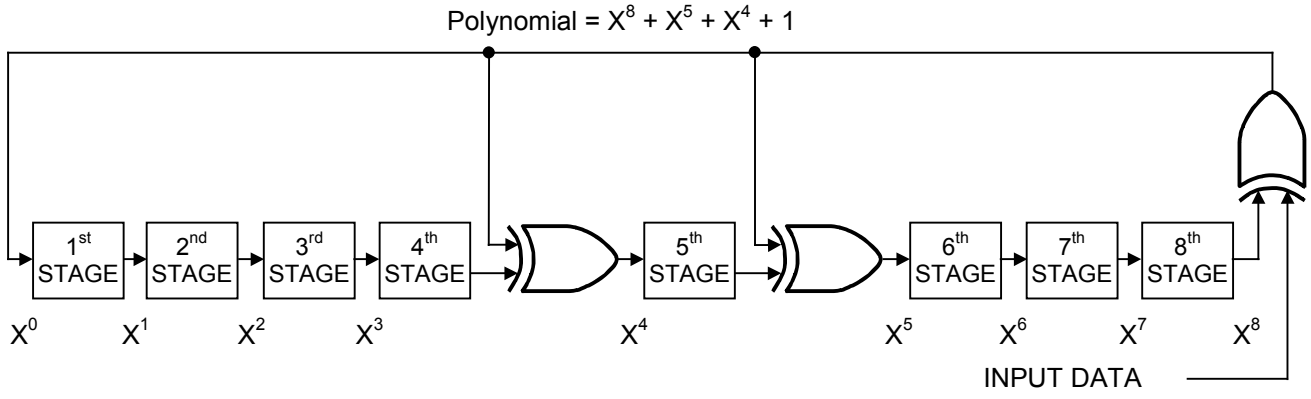


Figure 4. 1-Wire CRC Generator



MEMORY

The memory map of the DS1922L/T is shown in Figure 5. The 512 bytes general-purpose SRAM are located in pages 0 through 15. The various registers to set-up and control the device fill page 16 and 17, called register pages 1 and 2 (details in Figure 6). Pages 18 and 19 provide storage space for calibration data. They can alternatively be used as extension of the general-purpose memory. The "datalog" logging memory starts at address 1000h (page 128) and extends over 256 pages. The memory pages 20 to 127 are reserved for future extensions. The scratchpad is an additional page that acts as a buffer when writing to the SRAM memory or the register page. The data memory can be written at any time. The calibration memory holds data from the device calibration that can be used to further improve the accuracy of temperature readings. See the *Software Correction Algorithm for Temperature* section for details. While the calibration memory can be overwritten by the user, this is not recommended. See section *Security by Password* for ways to protect the memory. The access type for the register pages is register-specific and depends on whether the device is programmed for a mission. Figure 6 shows the details. The datalog memory is read-only for the user. It is written solely under supervision of the on-chip control logic. Due to the special behavior of the write access logic (write scratchpad, copy scratchpad) it is recommended to only write full pages at a time. This also applies to the register pages and the calibration memory. See the *Address Register and Transfer Status* section for details.

Figure 5. DS1922L/T Memory Map

	32-Byte Intermediate Storage Scratchpad	
ADDRESS		
0000H to 001FH	**32-Byte General-Purpose SRAM (R/W)**	Page 0
0020H to 01FFH	**General-Purpose SRAM (R/W)**	Pages 1 to 15
0200H to 021FH	**32-Byte Register Page 1**	Page 16
0220H to 023FH	**32-Byte Register Page 2**	Page 17
0240H to 025FH	**Calibration Memory Page 1 (R/W)**	Page 18
0260H to 027FH	**Calibration Memory Page 2 (R/W)**	Page 19
0280H to 0FFFH	(Reserved For Future Extensions)	Pages 20 to 127
1000H to 2FFFH	**Datalog Memory (Read-Only)**	Pages 128 to 383

Figure 6. DS1922L/T Register Pages Map

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	Function	Access*
0200h	0	10s			Single Seconds				Real-Time Clock Registers	R/W; R
0201h	0	10min.			Single Minutes					
0202h	0	12/24	20hr AM/PM	10hr	Single Hours					
0203h	0	0	10 Date		Single Date					
0204h	CENT	0	0	10m.	Single Months					
0205h	10yrs				Single Years					
0206h	Low Byte								Sample Rate	R/W; R
0207h	0	0	High Byte							
0208h	Low Threshold								Temp. Alarms	R/W; R
0209h	High Threshold									
020Ah	(no function with the DS1922L/T)								(N/A)	R/W; R
020Bh	(no function with the DS1922L/T)									
020Ch	Low Byte			0	0	0	0	0	Latest Temp.	R; R
020Dh	High Byte									
020Eh	(no function with the DS1922L/T)								(N/A)	R; R
020Fh	(no function with the DS1922L/T)									
0210h	0	0	0	0	0	0	ETHA	ETLA	T.Alm.En.	R/W; R
0211h	1	1	1	1	1	1	0	0	(N/A)	R/W; R
0212h	0	0	0	0	0	0	EHSS	EOSC	RTC En.	R/W; R
0213h	1	1	SUTA	RO	(X)	TLFS	0	ETL	Mis. Cntrl.	R/W; R
0214h	BOR	1	1	1	0	0	THF	TLF	Alm. Stat.	R; R
0215h	1	1	0	WFTA	MEMCLR	0	MIP	0	Gen. Stat.	R; R
0216h	Low Byte								Start Delay Counter	R/W; R
0217h	Center Byte									
0218h	High Byte									
0219h	0	10s			Single Seconds				Mission Time Stamp	R; R
021Ah	0	10min.			Single Minutes					
021Bh	0	12/24	20hr AM/PM	10hr	Single Hours					
021Ch	0	0	10 Date		Single Date					
021Dh	CENT	0	0	10m.	Single Months					
021Eh	10yrs				Single Years					
021Fh	(no function; reads 00h)								(N/A)	R; R
0220h	Low Byte								Mission Samples Counter	R; R
0221h	Center Byte									
0222h	High Byte									
0223h	Low Byte								Device Samples Counter	R; R
0224h	Center Byte									
0225h	High Byte									
0226h	Configuration Code								Flavor	R; R
0227h	EPW								PW. Cntrl.	R/W; R
0228h	First Byte								Read Access Password	W; ---
…	…									
022Fh	Eighth Byte									
0230h	First Byte								Full Access Password	W; —
…	…									
0237h	Eighth Byte									
0238h	(no function; all of these bytes read 00h)								(N/A)	R; R
…										
023Fh										

Note: The first entry in column ACCESS TYPE is valid between missions. The second entry shows the applicable access type while a mission is in progress.

TIMEKEEPING AND CALENDAR

The real-time clock (RTC)/alarm and calendar information is accessed by reading/writing the appropriate bytes in the register page, address 200h to 205h. For readings to be valid, all RTC registers must be read sequentially starting at address 0200h. Some of the RTC bits are set to 0. These bits will always read 0 regardless of how they are written. The number representation of the real-time clock registers is BCD format (binary-coded decimal).

Real-Time Clock and RTC Alarm Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0200h	0	10s			Single Seconds			
0201h	0	10min.			Single Minutes			
0202h	0	12/24	20hr AM/PM	10hr	Single Hours			
0203h	0	0	10 Date		Single Date			
0204h	CENT	0	0	10m.	Single Months			
0205h	10yrs				Single Years			

The RTC of the DS1922L/T can run in either 12-hour or 24-hour mode. Bit 6 of the Hours Register (address 202h) is defined as the 12- or 24-hour mode select bit. When high, the 12-hour mode is selected. In the 12-hour mode, bit 5 is the AM/PM bit with logic 1 being PM. In the 24-hour mode, bit 5 is the 20-hour bit (20 to 23 hours). The CENT bit, bit 7 of the Months Register, can be written by the user. This bit changes its state when the years counter transitions from 99 to 00.

The calendar logic is designed to automatically compensate for leap years. For every year value that is either 00 or a multiple of 4 the device will add a 29th of February. This will work correctly up to (but not including) the year 2100.

SAMPLE RATE

The content of the Sample Rate Register (addresses 0206h, 0207h) specifies the time elapse (in seconds if EHSS = 1, or minutes if EHSS = 0) between two temperature logging events. The sample rate may be any value from 1 to 16383, coded as an unsigned 14-bit binary number. If EHSS = 1, the shortest time between logging events is 1 second and the longest (sample rate = 3FFFh) is 4.55 hours. If EHSS = 0, the shortest is 1 minute and the longest time is 273.05 hours (sample rate = 3FFFh). The EHSS bit is located in the RTC Control Register at address 0212h. It is important that the user sets the EHSS bit accordingly while setting the Sample Rate Register. A sample rate of 0000h is not valid and must be avoided under all circumstances. This will cause the device to enter into an unrecoverable state.

Sample Rate Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0206h	Sample Rate Low							
0207h	0	0	Sample Rate High					

During a mission, there is only read access to these registers. Bits cells marked "0" always read 0 and cannot be written to 1.

TEMPERATURE CONVERSION

The DS1922L measures temperatures in the range of -40°C to +85°C. With the DS1922T the temperature range begins at 0°C and ends at +125°C. Temperature values are represented as a 8- or 16-bit unsigned binary number with a resolution of 0.5°C in the 8-bit mode and 0.0625°C in the 16-bit mode.

The higher temperature byte TRH is always valid. In the 16-bit mode only the three highest bits of the lower byte TRL are valid. The five lower bits all read zero. TRL is undefined if the device is in 8-bit temperature mode. An out-of-range temperature reading will be indicated as 00h or 0000h when too cold and FFh or FFE0h when too hot.

Latest Temperature Conversion Result Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	
020Ch	T2	T1	T0	0	0	0	0	0	**TRL**
020Dh	T10	T9	T8	T7	T6	T5	T4	T3	**TRH**

With TRH and TRL representing the decimal equivalent of a temperature reading the temperature value is calculated as

ϑ(°C) = TRH/2 - 41 + TRL/512 (16 bit mode, TLFS = 1, see address 0213h)
ϑ(°C) = TRH/2 - 41 (8 bit mode, TLFS = 0, see address 0213h)

This equation is valid for converting temperature readings stored in the datalog memory as well as for data read from the Latest Temperature Conversion Result Register. The "-41" applies to the DS1922L. For the DS1922T use "-1" instead of "-41".

To specify the temperature alarm thresholds, the equation above needs to be resolved to

TALM = 2 * ϑ (°C) + 82
The "+82" applies to the DS1922L. For the DS1922T use "+2" instead of "+82".

Since the temperature alarm threshold is only one byte, the resolution or temperature increment is limited to 0.5°C. The TALM value needs to be converted into hexadecimal format before it can be written to one of the temperature alarm threshold registers (**Low Alarm address 0208h; High Alarm address 0209h**). Independent of the conversion mode (8 or 16 bit) only the most significant byte of a temperature conversion is used to determine whether an alarm will be generated.

Temperature Conversion Examples

Mode	TRH		TRL		ϑ(°C)	ϑ(°C)
	hex	decimal	hex	decimal	DS1922L	DS1922T
8-bit	54h	**84**	—	—	1.0	41.0
8-bit	17h	**23**	—	—	-29.5	10.5
16-bit	54h	**84**	00h	**0**	1.000	41.000
16-bit	17h	**23**	60h	**96**	-29.3125	10.6875

Temperature Alarm Threshold Examples

ϑ(°C)	TALM (DS1922L)	
	hex	decimal
25.5	**85h**	133
-10.0	**3Eh**	62

ϑ(°C)	TALM (DS1922T)	
	hex	decimal
65.5	**85h**	133
30.0	**3Eh**	62

TEMPERATURE SENSOR ALARM

The DS1922L/T has two Temperature Alarm Threshold Registers (address 0208h, 0209h) to store values, which determine whether a critical temperature has been reached. A temperature alarm is generated if the device measures an alarming temperature AND the alarm signaling is enabled. The bits ETLA and ETHA that enable the temperature alarm are located in the Temperature Sensor Control Register. The temperature alarm flags TLF and THF are found in the Alarm Status Register at address 0214h.

Temperature Sensor Control Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0210h	0	0	0	0	0	0	ETHA	ETLA

During a mission, there is only read access to this register. Bits 2 to 7 have no function. They always read 0 and cannot be written to 1.

Register Details

BIT DESCRIPTION	BIT(S)	DEFINITION
ETLA: Enable Temperature Low Alarm	b0	This bit controls whether, during a mission, the temperature low alarm flag (TLF) may be set, if a temperature conversion results in a value equal to or lower than the value in the Temperature Low Alarm Threshold Register. If ETLA is 1, temperature low alarms are enabled. If ETLA is 0, temperature low alarms will not be generated.
ETHA: Enable Temperature High Alarm	b1	This bit controls whether, during a mission, the temperature high alarm flag (THF) may be set, if a temperature conversion results in a value equal to or higher than the value in the Temperature High Alarm Threshold Register. If ETHA is 1, temperature high alarms are enabled. If ETHA is 0, temperature high alarms will not be generated.

RTC CONTROL

To minimize the power consumption of a DS1922L/T, the RTC oscillator should be turned off when device is not in use. The oscillator on/off bit is located in the RTC control register. This register also includes the EHSS bit, which determines whether the sample rate is specified in seconds or minutes.

RTC Control Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0212h	0	0	0	0	0	0	EHSS	EOSC

During a mission, there is only read access to this register. Bits 2-7 have no function. They always read 0 and cannot be written to 1.

Register Details

BIT DESCRIPTION	BIT(S)	DEFINITION
EOSC: Enable Oscillator	b0	This bit controls the crystal oscillator of the real-time clock. When set to logic 1, the oscillator will start operation. When written to logic 0, the oscillator will stop and the device is in a low-power data retention mode. This bit must be 1 for normal operation. A temperature conversion must not be attempted while the RTC oscillator is stopped. This will cause the device to enter into an unrecoverable state.
EHSS: Enable High Speed Sample	b1	This bit controls the speed of the sample rate counter. When set to logic 0, the sample rate is specified in minutes. When set to logic 1, the sample rate is specified in seconds.

MISSION CONTROL

The DS1922L/T is set up for its operation by writing appropriate data to its special function registers, which are located in the two register pages. The settings in the Mission Control Register determine which format (8 or 16 bits) is to be used and whether old data may be overwritten by new data, once the datalog memory is full. An additional control bit can be set to tell the DS1922L/T to wait with logging data until a temperature alarm is encountered.

Mission Control Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0213h	1	1	SUTA	RO	(X)	TLFS	0	ETL

During a mission, there is only read access to this register. Bits 6 and 7 have no function. They always read 1 and cannot be written to 0. Bits 1 and 3 control functions that are not available with the DS1922L and DS1922T. Bit 1 must be set to 0. Under this condition the setting of bit 3 becomes a “don’t care”.

Register Details

BIT DESCRIPTION	BIT(S)	DEFINITION
ETL: Enable Temperature Logging	b0	To set up the device for a temperature-logging mission, this bit must be set to logic 1. The recorded temperature values will start at address 1000h.
TLFS: Temperature Logging Format Selection	b2	This bit specifies the format used to store temperature readings in the datalog memory. If this bit is 0, the data will be stored in 8-bit format. If this bit is 1, the 16-bit format will be used (higher resolution). With 16-bit format, the most-significant byte is stored at the lower address.
RO: Rollover Control	b4	This bit controls whether, during a mission, the datalog memory is overwritten with new data or whether data logging is stopped once the datalog memory is full. Setting this bit to 1 enables the rollover and data logging continues at the beginning, overwriting previously collected data. If this bit is 0, the logging and conversions will stop once the datalog memory is full. However, the RTC will continue to run and the MIP bit will remain set until the Stop Mission command is performed.
SUTA: Start Mission upon Temperature Alarm	b5	This bit specifies whether a mission begins immediately (includes delayed start) or if a temperature alarm will be required to start the mission. If this bit is 1, the device will perform an 8-bit temperature conversion at the selected sample rate and begin with data logging only if an alarming temperature (high alarm or low alarm) was found. The first logged temperature will be one sample period **after** the alarm occurred.

ALARM STATUS

The fastest way to determine whether a programmed temperature threshold was exceeded during a mission is through reading the Alarm Status Register. In a networked environment that contains multiple DS1922L/T iButtons the devices that encountered an alarm can quickly be identified by means of the Conditional Search command (see *ROM Function Commands*). The temperature alarm will only occur if enabled (*see Temperature Sensor Alarm*). The BOR alarm is always enabled.

Alarm Status Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0214h	BOR	1	1	1	0	0	THF	TLF

There is only read access to this register. Bits 4 to 6 have no function. They always read 1. Bits 2 and 3 have no function with the DS1922L and DS1922T. They always read 0. The alarm status bits are cleared simultaneously when the Clear Memory function is invoked. See *Memory and Control Functions* for details.

Register Details

BIT DESCRIPTION	BIT(S)	DEFINITION
TLF: Temperature Low Alarm Flag	b0	If this bit reads 1, there was at least one temperature conversion during a mission revealing a temperature equal to or lower than the value in the Temperature Low Alarm Register. A forced conversion can affect the TLF bit. This bit can also be set with the initial alarm in the SUTA = 1 mode.
THF: Temperature High Alarm Flag	b1	If this bit reads 1, there was at least one temperature conversion during a mission revealing a temperature equal to or higher than the value in the Temperature High Alarm Register. A forced conversion can affect the THF bit. This bit can also be set with the initial alarm in the SUTA = 1 mode.
BOR: Battery On Reset Alarm	b7	If this bit reads 1, the device has performed a power-on-reset. This indicates that the device has experienced a shock big enough to interrupt the internal battery power supply. The device may still appear functional, but it has lost its factory calibration. Any data found in the datalog memory should be disregarded.

GENERAL STATUS

The information in the general status register tells the host computer whether a mission-related command was executed successfully. Individual status bits indicate whether the DS1922L/T is performing a mission, waiting for a temperature alarm to trigger the logging of data or whether the data from the latest mission has been cleared.

General Status Register Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0215h	1	1	0	WFTA	MEMCLR	0	MIP	0

There is only read access to this register. Bits 0, 2, 5, 6, and 7 have no function.

Register Details

BIT DESCRIPTION	BIT(S)	DEFINITION
MIP: Mission In Progress	b1	If this bit reads 1 the device has been set up for a mission and this mission is still in progress. The MIP bit returns from logic 1 to logic 0 when a mission is ended. See function commands Start Mission and Stop Mission.
MEMCLR: Memory Cleared	b3	If this bit reads 1, the Mission Time Stamp, Mission Samples Counter, as well as all the alarm flags of the Alarm Status Register have been cleared in preparation of a new mission. Executing the Clear Memory command clears these memory sections. The MEMCLR bit will return to 0 as soon as a new mission is started by using the Start Mission command. The memory has to be cleared in order for a mission to start.
WFTA: Waiting for Temperature Alarm	b4	If this bit reads 1, the Mission Start upon Temperature Alarm was selected and the Start Mission command was successfully executed, but the device has not yet experienced the temperature alarm. This bit is cleared after a temperature alarm event, but is not affected by the Clear Memory command. Once set, WFTA will remain set if a mission is stopped before a temperature alarm occurs. To clear WFTA manually before starting a new mission, set the high temperature alarm (address 0209h) to -40°C and perform a forced conversion.

MISSION START DELAY

The content of the Mission Start Delay Counter tells how many minutes will have to expire from the time a mission was started until the first measurement of the mission will take place (SUTA = 0) or until the device will start testing the temperature for a temperature alarm (SUTA = 1). The Mission Start Delay is stored as an unsigned 24-bit integer number. The maximum delay is 16777215 minutes, equivalent to 11650 days or roughly 31 years. If the start delay is non-zero and the SUTA bit is set to 1, first the delay has to expire before the device starts testing for temperature alarms to begin logging data.

Mission Start Delay Counter

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0216h	Delay Low Byte							
0217h	Delay Center Byte							
0218h	Delay High Byte							

During a mission, there is only read access to these registers.

For a typical mission, the Mission Start Delay is 0. If a mission is too long for a single DS1922L/T to store all readings at the selected sample rate, one can use several devices and set the Mission Start Delay for the second device to start recording as soon as the memory of the first device is full, and so on. The RO-bit in the Mission Control Register (address 0213h) must be set to 0 to prevent overwriting of collected data once the datalog memory is full.

MISSION TIME STAMP

The Mission Time Stamp indicates the date and time of the first temperature sample of the mission. There is only read access to the Mission Time Stamp Register.

Mission Time Stamp Registers Bitmap

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0219h	0	10s			Single Seconds			
021Ah	0	10min.			Single Minutes			
021Bh	0	12/24	20hr AM/PM	10hr	Single Hours			
021Ch	0	0	10 Date		Single Date			
021Dh	CENT	0	0	10m.	Single Months			
021Eh	10yrs				Single Years			

MISSION PROGRESS INDICATOR

Depending on settings in the Mission Control Register (address 0213h) the DS1922L/T will log temperature in 8-bit or 16-bit format. The Mission Samples Counter together with the starting address and the logging format (8 or 16 bits) provides the information to identify valid blocks of data that have been gathered during the current (MIP = 1) or latest mission (MIP = 0). See *Datalog Memory Usage* for an illustration.

Mission Samples Counter Register Map

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0220h	Low Byte							
0221h	Center Byte							
0222h	High Byte							

There is only read access to this register.

The number read from the Mission Samples Counter indicates how often the DS1922L/T woke up during a mission to measure temperature. The number format is 24-bit unsigned integer. The Mission Samples Counter is reset through the Clear Memory command.

OTHER INDICATORS

The Device Samples Counter is similar to the Mission Samples Counter. During a mission this counter increments whenever the DS1922L/T wakes up to measure and log data and when the device is testing for a temperature alarm in SUTA mode. Between missions the counter increments whenever the Forced Conversion command is executed. This way the Device Samples Counter functions like a gas gauge for the battery that powers the iButton.

Device Samples Counter Register Map

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0223h	Low Byte							
0224h	Center Byte							
0225h	High Byte							

There is only read access to this register.

The Device Samples Counter is reset to zero when the iButton is assembled. The counter will increment a couple of times during final test. The number format is 24-bit unsigned integer. The maximum number that can be represented in this format is 16777215.

The Device Configuration Byte is used to allow the master to distinguish between the DS2422 chip, and different versions of the DS1922 iButtons. The table below shows the codes assigned to the various devices.

Device Configuration Byte

ADDR	b7	b6	b5	b4	b3	b2	b1	b0	
0226h	0	0	0	0	0	0	0	0	DS2422
0226h	0	1	0	0	0	0	0	0	DS1922L
0226h	0	1	1	0	0	0	0	0	DS1922T

There is only read access to this register.

SECURITY BY PASSWORD

The DS1922L/T is designed to use two passwords that control read access and full access. Reading from or writing to the scratchpad as well as the forced conversion command does not require a password. The password needs to be transmitted right after the command code of the memory or control function. If password checking is enabled the password transmitted is compared to the passwords stored in the device. The data pattern stored in the Password Control register determines whether password checking is enabled.

Password Control Register

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0227h	EPW							

During a mission, there is only read access to this register.

To enable password checking, the EPW bits need to form a binary pattern of 10101010 (AAh). The default pattern of EPW is different from AAh. If the EPW pattern is different from AAh, any pattern will be accepted, as long as it has a length of exactly 64 bits. Once enabled, changing the passwords and disabling password checking requires the knowledge of the current full-access password.

Before enabling password checking, passwords for read-only access as well as for full access (read/write/control) need to be written to the password registers. Setting up a password or enabling/disabling the password checking is done in the same way as writing data to a memory location, only the address is different. Since they are located in the same memory page, both passwords can be redefined at the same time.

Read Access Password Register

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0228h	RP7	RP6	RP5	RP4	RP3	RP2	RP1	RP0
0229h	RP15	RP14	RP13	RP12	RP11	RP10	RP9	RP8
—				…				—
022Eh	RP55	RP54	RP53	RP52	RP51	RP50	RP49	RP48
022Fh	RP63	RP62	RP61	RP60	RP59	RP58	RP57	RP56

There is only write access to this register. Attempting to read the password will report all zeros. The password cannot be changed while a mission is in progress.

The Read Access Password needs to be transmitted exactly in the sequence RP0, RP1… RP62, RP63. This password only applies to the function “Read Memory with CRC”. The DS1922L/T will deliver the requested data only if the password transmitted by the master was correct or if password checking is not enabled.

Full Access Password Register

ADDR	b7	b6	b5	b4	b3	b2	b1	b0
0230h	FP7	FP6	FP5	FP4	FP3	FP2	FP1	FP0
0231h	FP15	FP14	FP13	FP12	FP11	FP10	FP9	FP8
—				—				—
0236h	FP55	FP54	FP53	FP52	FP51	FP50	FP49	FP48
0237h	FP63	FP62	FP61	FP60	FP59	FP58	FP57	FP56

There is only write access to this register. Attempting to read the password will report all zeros. The password cannot be changed while a mission is in progress.

The Full Access Password needs to be transmitted exactly in the sequence FP0, FP1… FP62, FP63. It will affect the functions “Read Memory with CRC”, “Copy Scratchpad”, “Clear Memory”, “Start Mission”, and “Stop Mission”. The DS1922L/T executes the command only if the password transmitted by the master was correct or if password checking is not enabled

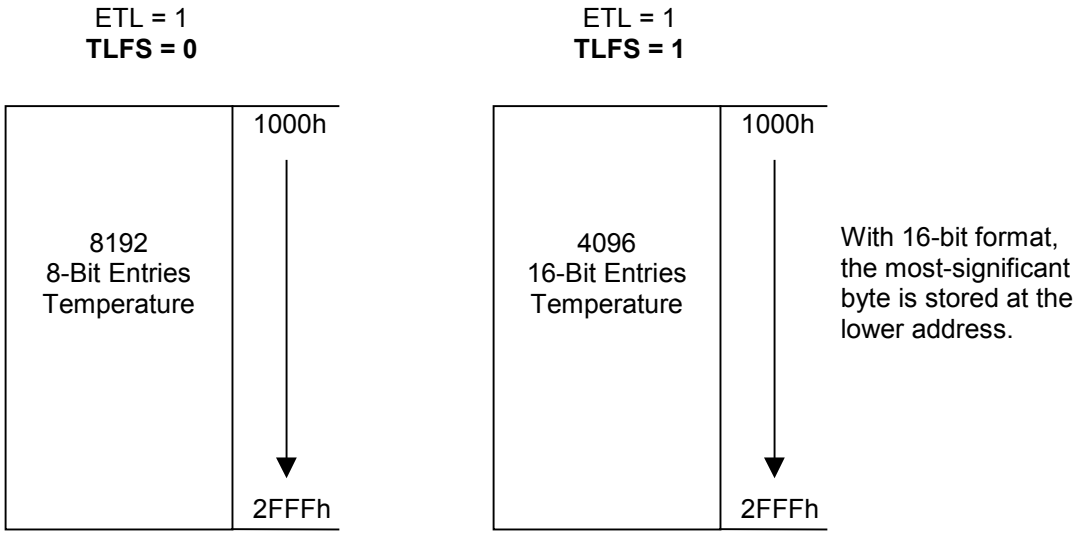
Due to the special behavior of the write access logic, the Password Control Register and both passwords must be written at the same time. When setting up new passwords, always verify (read back) the scratchpad before sending the copy scratchpad command. After a new password is successfully copied from the scratchpad to its memory location, erase the scratchpad by filling it with new data (write scratchpad command). Otherwise a copy of the passwords will remain in the scratchpad for public read access.

DATALOG MEMORY USAGE

Once setup for a mission, the DS1922L/T logs the temperature measurements at equidistant time points entry after entry in its datalog memory. The datalog memory is able to store 8192 entries in 8-bit format or 4096 entries in 16-bit format (Figure 7). In 16-bit format, the higher 8 bits of an entry are stored at the lower address. Knowing the starting time point (Mission Time Stamp) and the interval between temperature measurements one can reconstruct the time and date of each measurement.

There are two alternatives to the way the DS1922L/T will behave after the datalog memory is filled with data. The user can program the device to either stop any further recording (disable “rollover”) or overwrite the previously recorded data (enable “rollover”), one entry at a time, starting again at the beginning of the respective memory section. The contents of the Mission Samples Counter in conjunction with the sample rate and the Mission Time Stamp will then allow reconstructing the time points of all values stored in the datalog memory. This gives the exact history over time for the most recent measurements taken. Earlier measurements cannot be reconstructed.

Figure 7. Temperature Logging



MISSIONING

The typical task of the DS1922L/T iButton is recording temperature. Before the device can perform this function, it needs to be set up properly. This procedure is called missioning.

First of all, DS1922L/T needs to have its real-time clock set to valid time and date. This reference time may be the local time, or, when used inside of a mobile unit, UTC (also called GMT, Greenwich Mean Time) or any other time standard that was agreed upon. The real-time clock oscillator must be running (EOSC = 1). The memory assigned to store the Mission Time Stamp, Mission Samples Counter, and Alarm Flags must be cleared using the Memory Clear command. To enable the device for a mission, the ETL-bit must be set to 1. These are general settings that have to be made in any case, regardless of the type of object to be monitored and the duration of the mission.

If alarm signaling is desired, the temperature alarm low and high thresholds must be defined. How to convert a temperature value into the binary code to be written to the threshold registers is described under *Temperature Conversion* earlier in this document. In addition, the temperature alarm must be enabled for the low- and/or high-threshold. This makes the device respond to a Conditional Search command (see *ROM Function Commands*), provided that an alarming condition has been encountered.

The setting of the RO bit (rollover enable) and sample rate depends on the duration of the mission and the monitoring requirements. If the most recently logged data is important, the rollover should be enabled (RO = 1). Otherwise one should estimate the duration of the mission in minutes and divide the number by 8192 (8-bit format) or 4096 (16-bit format) to calculate the value of the sample rate (number of minutes between conversions). If the estimated duration of a mission is 10 days (= 14400 minutes), for example, then the 8192-byte capacity of the datalog memory would be sufficient to store a new 8-bit value every 1.8 minutes (110 seconds). If the datalog memory of the DS1922L/T is not large enough to store all readings, one can use several devices and set the Mission Start Delay to values that make the second device start logging as soon as the memory of the first device is full, and so on. The RO bit needs to be set to 0 to disable rollover that would otherwise overwrite the logged data.

After the RO bit and the Mission Start Delay are set, the sample rate needs to be written to the Sample Rate Register. The sample rate may be any value from 1 to 16383, coded as an unsigned 14-bit binary number. A sample rate of all zeros is not valid and must be avoided under all circumstances. This will cause the device to enter into an unrecoverable state. The fastest sample rate is one sample per second (EHSS = 1, Sample Rate = 0001h) and the slowest is one sample every 273.05 hours (EHSS = 0, Sample Rate = 3FFFh). To get one sample every 6 minutes, for example, the sample rate value needs to be set to 6 (EHSS = 0) or 360 decimal (equivalent to 0168h at EHSS = 1).

If there is a risk of unauthorized access to the DS1922L/T or manipulation of data, one should define passwords for read access and full access. Before the passwords become effective, their use needs to be enabled. See Security by Password for more details.

The last step to begin a mission is to issue the Start Mission command. As soon as it has received this command, the DS1922L/T sets the MIP flag and clear the MEMCLR flag. With the immediate/delayed start mode (SUTA = 0), after as many minutes as specified by the Mission Start Delay are over, the device will wake up, copy the current date and time to the mission time stamp register, and log the first entry of the mission. This increments both the Mission Samples Counter and Device Samples Counter. All subsequent log entries will be made as specified by the value in the Sample Rate Register and the EHSS bit.

If the Start Upon Temperature Alarm mode is chosen (SUTA = 1) and temperature logging is enabled (ETL = 1) the DS1922L/T first waits until the start delay is over. Then the device wakes up in intervals as specified by the sample rate and EHSS bit and measure the temperature. This will increment the Device Samples Counter only. Only after an alarming temperature is encountered will the DS1922L/T set the mission time stamp. The first sample of the mission is logged one sample period after the temperature alarm occurred. From then on, both the Mission Samples Counter and Device Samples Counter increment at the same time. All subsequent log entries are made as specified by the value in the Sample Rate Register and the EHSS bit.

The general-purpose memory operates independently of the other memory sections and is not write-protected during a mission. All memory of the DS1922L/T can be read at any time, e. g., to watch the progress of a mission. Attempts to read the passwords will read 00h bytes instead of the data that is stored in the password registers.

ADDRESS REGISTERS AND TRANSFER STATUS

Because of the serial data transfer, the DS1922L/T employs three address registers, called TA1, TA2, and E/S (Figure 8). Registers TA1 and TA2 must be loaded with the target address to which the data are written or from which data are sent to the master upon a Read command. Register E/S acts like a byte counter and transfer status register. It is used to verify data integrity with Write commands. Therefore, the master only has read access to this register. The lower 5 bits of the E/S Register indicate the address of the last byte that has been written to the scratchpad. This address is called Ending Offset. **The DS1922L/T requires that the Ending Offset is always 1Fh for a Copy Scratchpad to function.** Bit 5 of the E/S Register, called PF or "partial byte flag," is set if the number of data bits sent by the master is not an integer multiple of 8. Bit 6 is always a 0. Note that the lowest 5 bits of the target address also determine the address within the scratchpad, where intermediate storage of data begins. This address is called byte offset. If the target address for a Write command is 13Ch, for example, then the scratchpad stores incoming data beginning at the byte offset 1Ch and will be full after only 4 bytes. The corresponding ending offset in this example is 1Fh. For best economy of speed and efficiency, the target address for writing should point to the beginning of a page, i.e., the byte offset will be 0. Thus the full 32-byte capacity of the scratchpad is available, resulting also in the ending offset of 1Fh. The ending offset together with the PF is mainly a means to support the master checking the data integrity after a Write command. The highest valued bit of the E/S Register, called AA or Authorization Accepted, indicates that a valid copy command for the scratchpad has been received and executed. Writing data to the scratchpad clears this flag.

Figure 8. Address Registers

Bit #	7	6	5	4	3	2	1	0
Target Address (TA1)	T7	T6	T5	T4	T3	T2	T1	T0
Target Address (TA2)	T15	T14	T13	T12	T11	T10	T9	T8
Ending Address with Data Status (E/S) (Read Only)	AA	0	PF	E4	E3	E2	E1	E0

WRITING WITH VERIFICATION

To write data to the DS1922L/T, the scratchpad has to be used as intermediate storage. First the master issues the Write Scratchpad command to specify the desired target address, followed by the data to be written to the scratchpad. In the next step, the master sends the Read Scratchpad command to read the scratchpad and to verify data integrity. As preamble to the scratchpad data, the DS1922L/T sends the requested target address TA1 and TA2 and the contents of the E/S Register. If the PF flag is set, data did not arrive correctly in the scratchpad. The master does not need to continue reading; it can start a new trial to write data to the scratchpad. Similarly, a set AA flag indicates that the Write command was not recognized by the device. If everything went correctly, both flags are cleared and the ending offset indicates the address of the last byte written to the scratchpad. Now the master can continue verifying every data bit. After the master has verified the data, it has to send the Copy Scratchpad command. This command must be followed exactly by the data of the three address registers TA1, TA2, and E/S as the master has read them verifying the scratchpad. As soon as the DS1922L/T has received these bytes, it copies the data to the requested location beginning at the target address.

MEMORY- AND CONTROL-FUNCTION COMMANDS

The Memory/Control Function Flow Chart (Figure 9) describes the protocols necessary for accessing the memory and the special function registers of the DS1922L/T. An example on how to use these and other functions to set up the DS1922L/T for a mission is included at the end of this document, preceding the Electrical Characteristics section. The communication between master and DS1922L/T takes place either at regular speed (default, OD = 0) or at Overdrive Speed (OD = 1). If not explicitly set into the Overdrive mode the DS1922L/T assumes regular speed. Internal memory access during a mission has priority over external access through the 1-Wire interface. This affects several of the commands described below. See section *Memory Access Conflicts* for details and remedies.

WRITE SCRATCHPAD COMMAND [0FH]

After issuing the Write Scratchpad command, the master must first provide the 2-byte target address, followed by the data to be written to the scratchpad. The data is written to the scratchpad starting at the byte offset (T4:T0). The master has to send as many bytes as are needed to reach the Ending Offset of 1Fh. If a data byte is incomplete, its content is ignored and the partial byte flag PF is set.

When executing the Write Scratchpad command the CRC generator inside the DS1922L/T (see Figure 15) calculates a CRC of the entire data stream, starting at the command code and ending at the last data byte sent by the master. This CRC is generated using the CRC16 polynomial by first clearing the CRC generator and then shifting in the command code (0Fh) of the Write Scratchpad command, the target addresses TA1 and TA2 as supplied by the master and all the data bytes. If the ending offset is 11111b, the master may send 16 read time slots and receive the inverted CRC16 generated by the DS1922L/T.

Note that both register pages are write-protected during a mission. Although the Write Scratchpad command works normally at any time, the subsequent copy scratchpad to a register page will fail during a mission.

READ SCRATCHPAD COMMAND [AAH]

This command is used to verify scratchpad data and target address. After issuing the Read Scratchpad command, the master begins reading. The first 2 bytes will be the target address. The next byte is the ending offset/data status byte (E/S) followed by the scratchpad data beginning at the byte offset (T4:T0), as shown in Figure 8. The master may continue reading data until the end of the scratchpad after which it receives an inverted CRC16 of the command code, Target Addresses TA1 and TA2, the E/S byte, and the scratchpad data starting at the target address. After the CRC is read, the bus master reads logical 1s from the DS1922L/T until a reset pulse is issued.

COPY SCRATCHPAD WITH PASSWORD [99H]

This command is used to copy data from the scratchpad to the writable memory sections. After issuing the Copy Scratchpad command, the master must provide a 3-byte authorization pattern, which can be obtained by reading the scratchpad for verification. This pattern must exactly match the data contained in the three address registers (TA1, TA2, E/S, in that order). Next the master must transmit the 64-bit full-access password. If passwords are enabled and the transmitted password is different from the stored full-access password, the Copy Scratchpad with Password command will fail. The device will stop communicating and will wait for a reset pulse. If the password was correct or if passwords were not enabled, the device will test the 3-byte authorization code. If the authorization code pattern matches, the AA (Authorization Accepted) flag will be set and the copy will begin. A pattern of alternating 1s and 0s will be transmitted after the data has been copied until the master issues a reset pulse. While the copy is in progress any attempt to reset the part will be ignored. Copy typically takes 2µs per byte.

The data to be copied is determined by the three address registers. The scratchpad data from the beginning offset through the ending offset will be copied, starting at the target address. The AA flag will remain at logic 1 until it is cleared by the next Write Scratchpad command. With suitable password, the copy scratchpad always functions for the 16 pages of data memory and the 2 pages of calibration memory. While a mission is in progress, write attempts to the register pages are not successful. The AA bit (Authorization Accepted) remaining at 0 indicates this.

Figure 9-1. Memory/Control Function Flow Chart

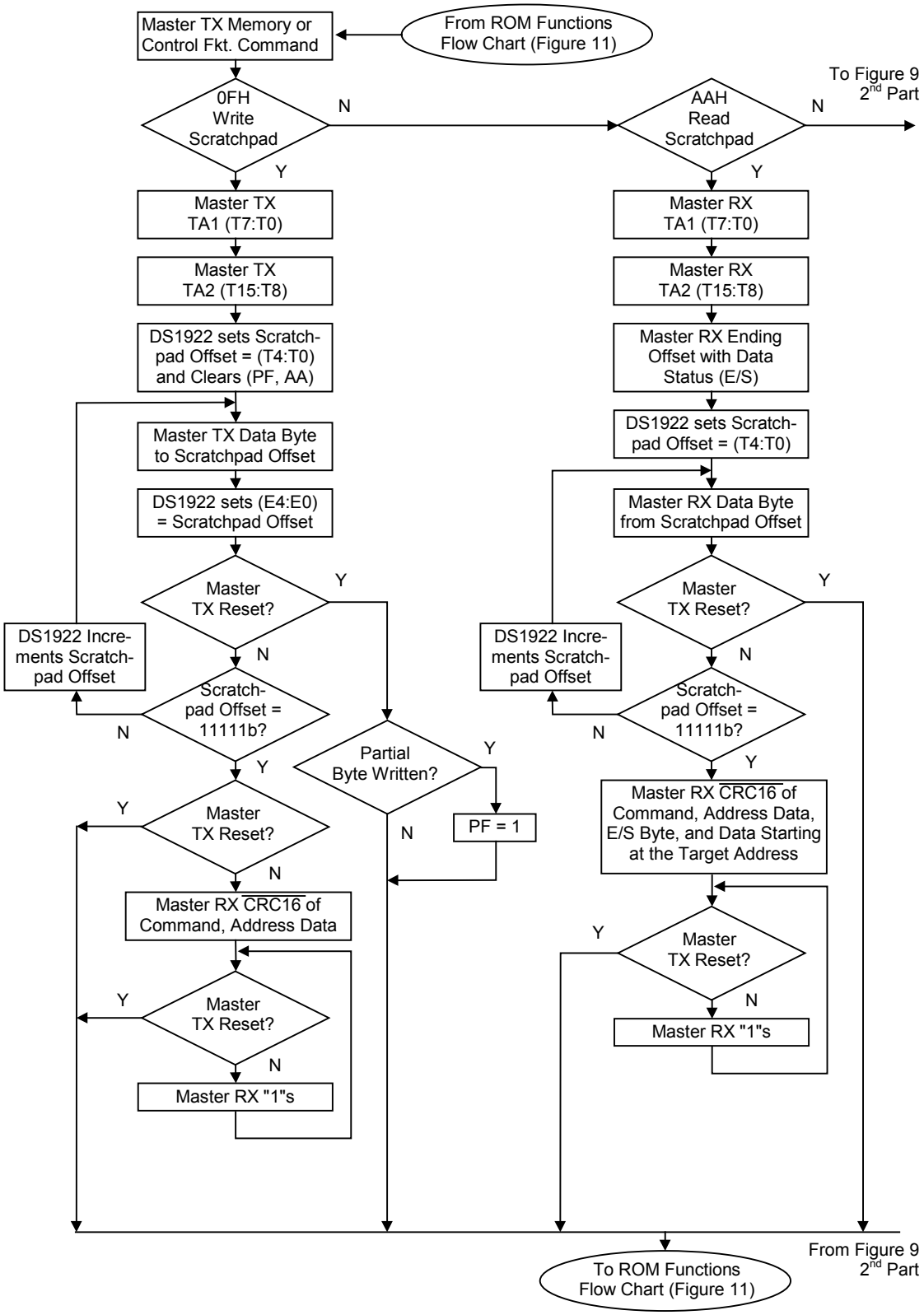


Figure 9-2. Memory/Control Function Flow Chart

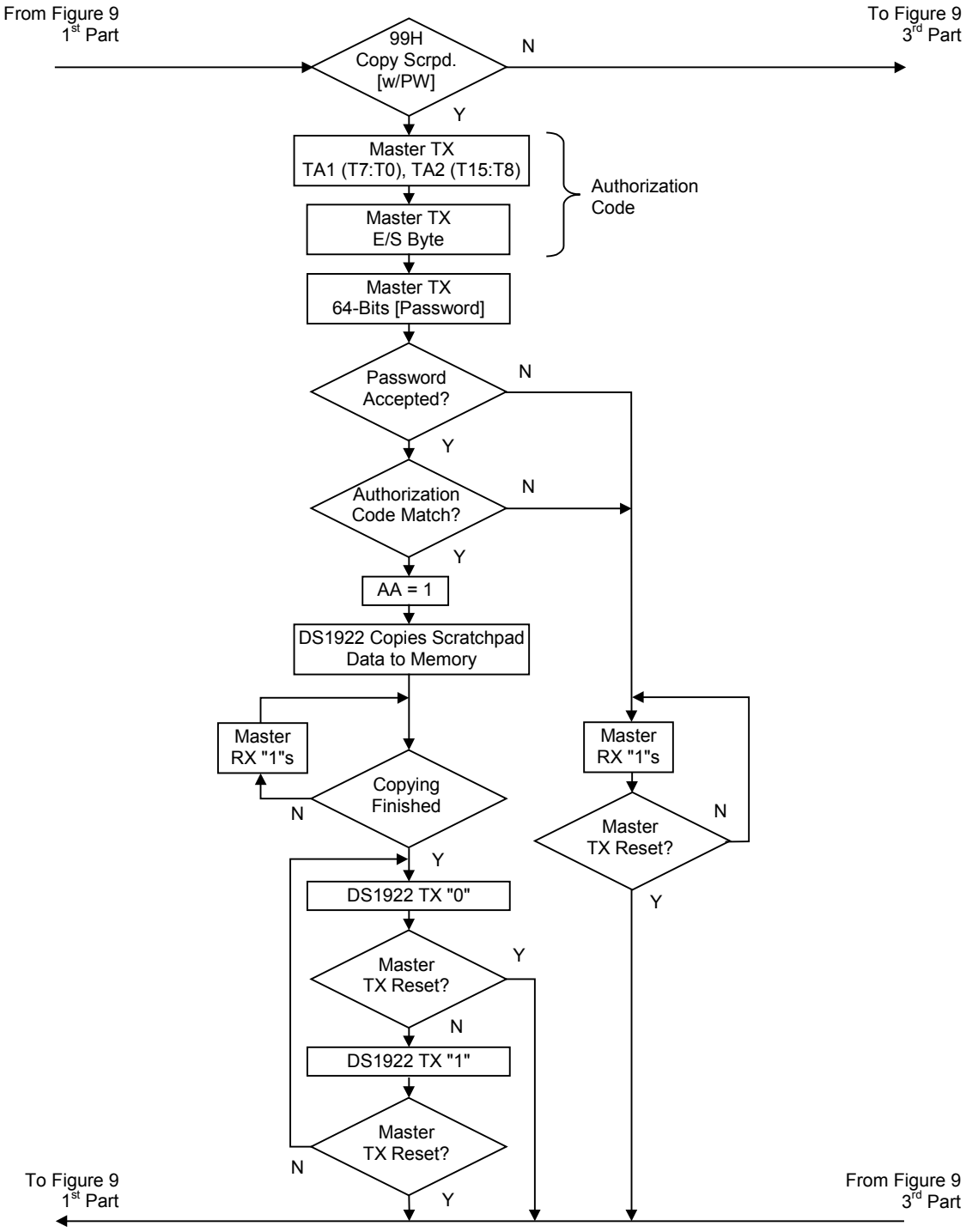


Figure 9-3. Memory/Control Function Flow Chart

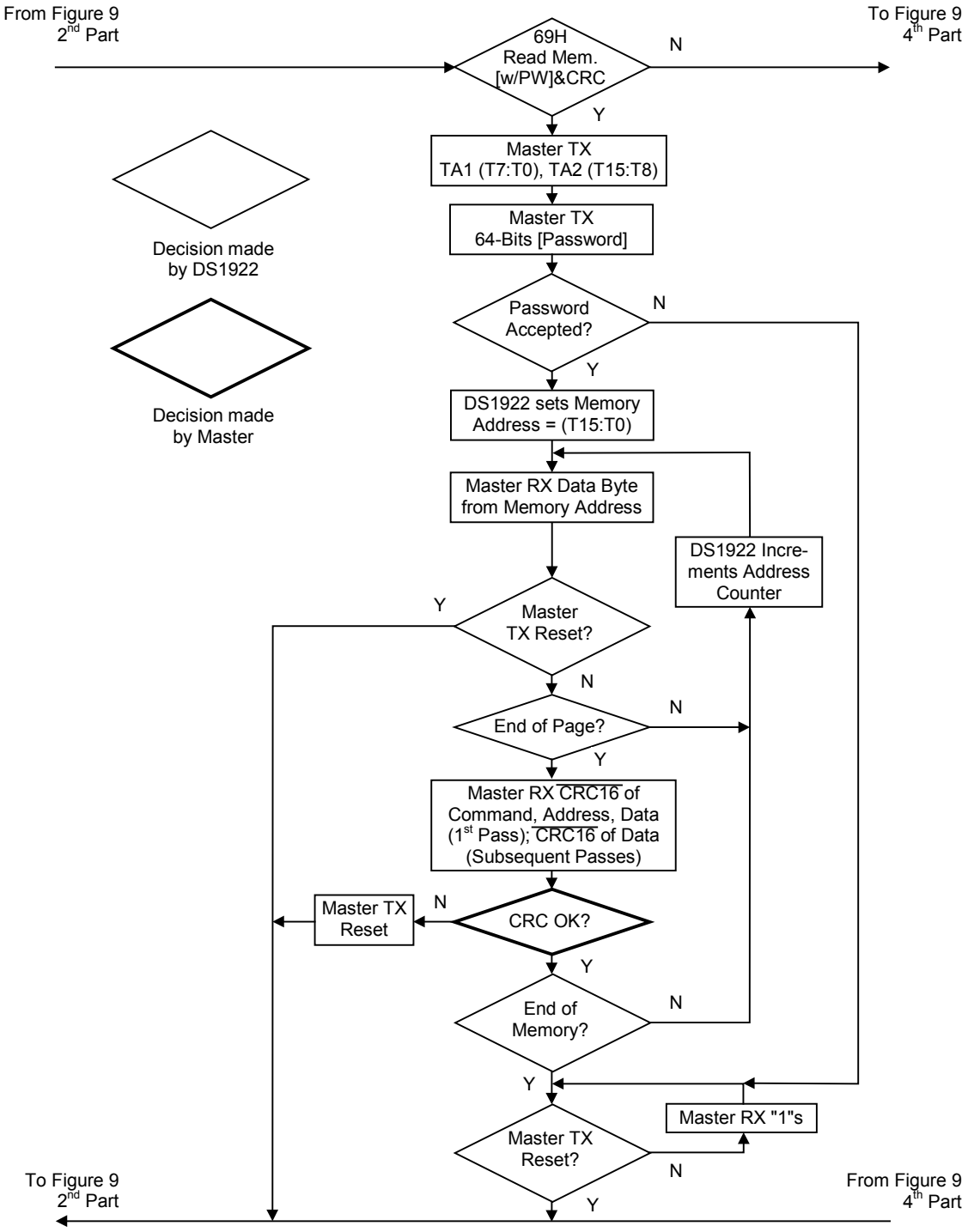


Figure 9-4. Memory/Control Function Flow Chart

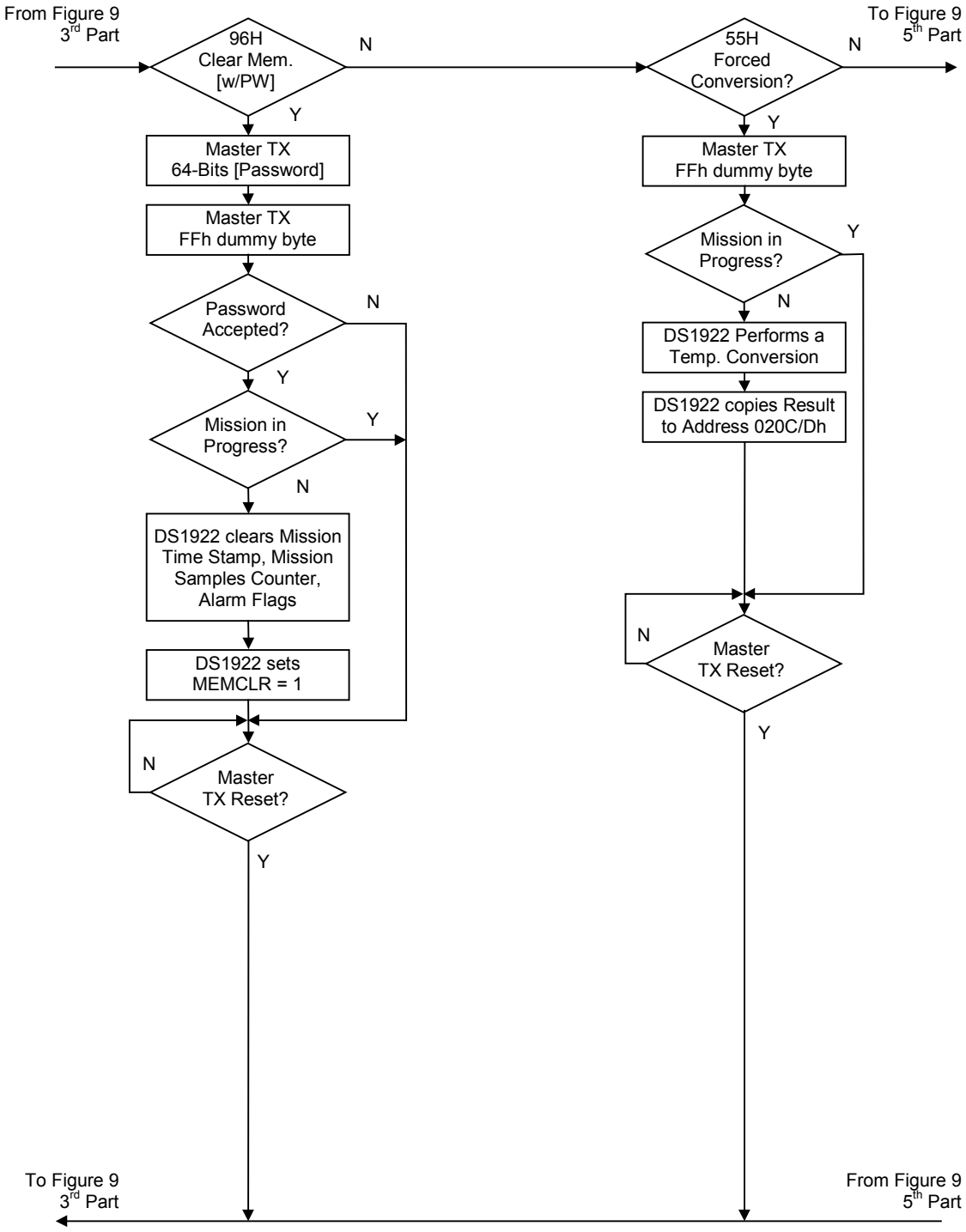
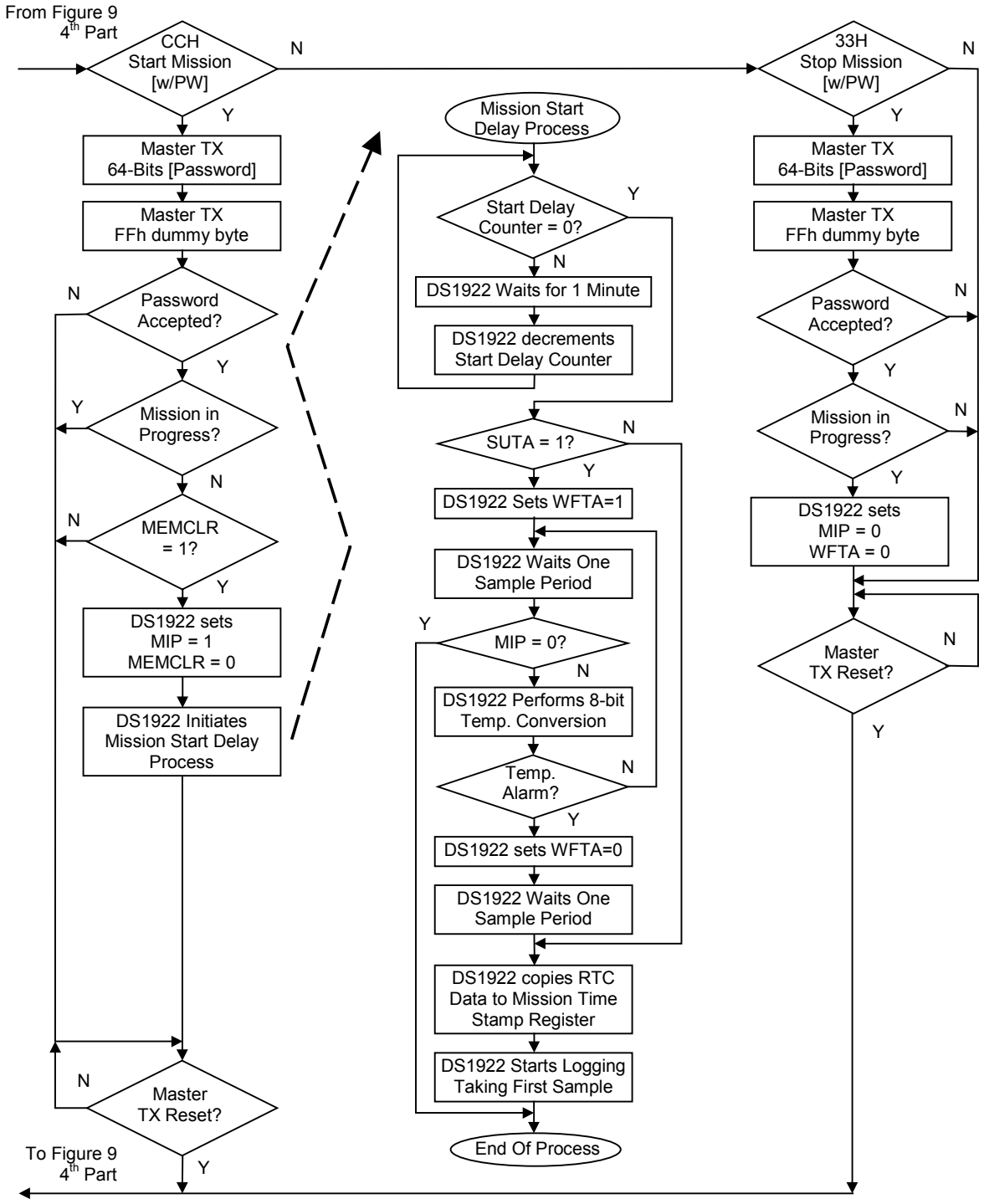


Figure 9-5. Memory/Control Function Flow Chart



READ MEMORY WITH PASSWORD AND CRC [69H]

The Read Memory with CRC command is the general function to read from the device. This command generates and transmits a 16-bit CRC following the last data byte of a memory page.

After having sent the command code of the Read Memory with CRC command, the bus master sends a 2-byte address that indicates a starting byte location. Next the master must transmit one of the 64-bit passwords. If passwords are enabled and the transmitted password does not match one of the stored passwords, the Read Memory with Password and CRC command will fail. The device will stop communicating and will wait for a reset pulse. If the password was correct or if passwords were not enabled, the master reads data from the DS1922L/T beginning from the starting address and continuing until the end of a 32-byte page is reached. At that point the bus master will send 16 additional read data time slots and receive the inverted 16-bit CRC. With subsequent read data time slots the master will receive data starting at the beginning of the next memory page followed again by the CRC for that page. This sequence will continue until the bus master resets the device. When trying to read the passwords or memory areas that are marked as "reserved", the DS1922L/T will transmit 00h or FFh bytes respectively. The CRC at the end of a 32-byte memory page is based on the data as it was transmitted.

With the initial pass through the Read Memory with CRC flow, the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator followed by the 2 address bytes and the contents of the data memory. Subsequent passes through the Read Memory with CRC flow will generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the contents of the data memory page. After the 16-bit CRC of the last page is read, the bus master will receive logical 1s from the DS1922L/T until a reset pulse is issued. The Read Memory with CRC command sequence can be ended at any point by issuing a reset pulse.

CLEAR MEMORY WITH PASSWORD [96H]

The Clear Memory with Password command is used to prepare the device for another mission. This command is only executed if no mission is in progress. After the command code the master must transmit the 64-bit full-access password followed by a FFh dummy byte. If passwords are enabled and the transmitted password is different from the stored full-access password or a mission is in progress, the Clear Memory with Password command will fail. The device will stop communicating and will wait for a reset pulse. If the password was correct or if passwords were not enabled, the device will clear the Mission Time Stamp, Mission Samples Counter, and all alarm flags of the Alarm Status Register. After these cells are cleared, the MEMCLR bit of the General Status Register will read 1 to indicate the successful execution of the Clear Memory with Password command. Clearing of the datalog memory is not necessary because the Mission Samples Counter indicates how many entries in the datalog memory are valid.

FORCED CONVERSION [55H]

The Forced Conversion command can be used to measure the temperature without starting a mission. After the command code the master has to send one FFh byte to get the conversion started. The conversion result is found as 16-bit value in the Latest Temperature Conversion Result register. This command is only executed if no mission is in progress (MIP = 0). It cannot be interrupted and takes maximum 600 ms to complete. During this time memory access through the 1-Wire interface is blocked. The device will behave the same way as during a mission when the sampling interferes with a memory/control function command. See section *Memory Access Conflicts* for details. A forced conversion must not be attempted while the RTC oscillator is stopped. This will cause the device to enter into an unrecoverable state.

START MISSION WITH PASSWORD [CCH]

The DS1922L/T uses a control function command to start a mission. A new mission can only be started if the previous mission has been ended and the memory has been cleared. After the command code, the master must transmit the 64-bit full-access password followed by a FFh dummy byte. If passwords are enabled and the transmitted password is different from the stored full-access password or a mission is in progress, the Start Mission with Password command will fail. The device will stop communicating and will wait for a reset pulse. If the password was correct or if passwords were not enabled, the device will start a mission. The sampling and data logging will begin as soon as the mission start delay is over (SUTA = 0) and, if SUTA = 1, one sample period after a temperature alarm was encountered. While the device is waiting for a temperature alarm to occur, the WFTA flag in the general status register will read 1. During a mission there is only read access to the Register Pages.

STOP MISSION WITH PASSWORD [33H]

The DS1922L/T uses a control function command to stop a mission. Only a mission that is in progress can be stopped. After the command code, the master must transmit the 64-bit full-access password followed by a FFh dummy byte. If passwords are enabled and the transmitted password is different from the stored full-access password or a mission is not in progress, the Stop Mission with Password command will fail. The device will stop communicating and will wait for a reset pulse. If the password was correct or if passwords were not enabled, the device will clear the MIP bit in the General Status Register and restore write access to the Register Pages. The WFTA bit is not cleared. See the description of the General Status Register for a method to clear the WFTA bit.

MEMORY ACCESS CONFLICTS

While a mission is in progress or while the device is waiting for a temperature alarm to start a mission, periodically a temperature sample is taken and logged. This "internal activity" has priority over 1-Wire communication. As a consequence, device-specific commands (excluding ROM function commands and 1-Wire reset) will not perform properly when internal and "external" activities interfere with each other. Not affected are the commands Start Mission, Forced Conversion and Clear Memory, because they are not applicable while a mission is in progress or while the device is waiting for a temperature alarm. The table below explains how the remaining five commands are affected by internal activity, how to detect this interference and how to work around it.

COMMAND	INDICATION OF INTERFERENCE	REMEDY
Write Scratchpad	The CRC16 at the end of the command flow reads FFFFh.	Wait 0.5 s, 1-Wire reset, address the device, repeat Write Scratchpad with the same data and check the validity of the CRC16 at the end of the command flow. Alternatively, use Read Scratchpad to verify data integrity.
Read Scratchpad	The data read changes to FFh bytes or all bytes received are FFh, including the CRC at the end of the command flow.	Wait 0.5s, 1-Wire reset, address the device, repeat Read Scratchpad and check the validity of the CRC16 at the end of the command flow.
Copy Scratchpad	The device behaves as if Authorization Code or pass-word was not valid or as if the copy function would not end.	Wait 0.5s, 1-Wire reset, address the device, issue Read Scratchpad and check the AA-bit of the E/S byte. If the AA-bit is set, Copy Scratchpad was successful.
Read Memory with CRC	The data read changes to all FFh bytes or all bytes received are FFh, including the CRC at the end of the command flow, despite a valid password.	Wait 0.5s, 1-Wire reset, address the device, repeat Read Memory with CRC and check the validity of the CRC16 at the end of the memory page.
Stop Mission	The general Status register at address 215h reads FFh or the MIP bit is 1 while bits 0, 2, and 5 are 0.	Wait 0.5s, 1-Wire reset, address the device, and repeat Stop Mission. Perform a 1-Wire reset, address the device, read the general Status register at address 215h and check the MIP-bit. If the MIP-bit is 0, Stop Mission was successful.

The interference is more likely to be seen with a high sample rate (1 sample every second) and with high-resolution logging, which can last up to 600ms. With lower sample rates interference may hardly be visible at all. In any case, when writing driver software, it is important to know about the possibility of interference and to take measures to work around it.

1-Wire BUS SYSTEM

The 1-Wire bus is a system, which has a single bus master and one or more slaves. In all instances the DS1922L/T is a slave device. The bus master is typically a microcontroller. The discussion of this bus system is broken down into three topics: hardware configuration, transaction sequence, and 1-Wire signaling (signal types and timing). The 1-Wire protocol defines bus transactions in terms of the bus state during specific time slots that are initiated on the falling edge of sync pulses from the bus master. For a more detailed protocol description, refer to Chapter 4 of the *Book of DS19xx iButton Standards*.

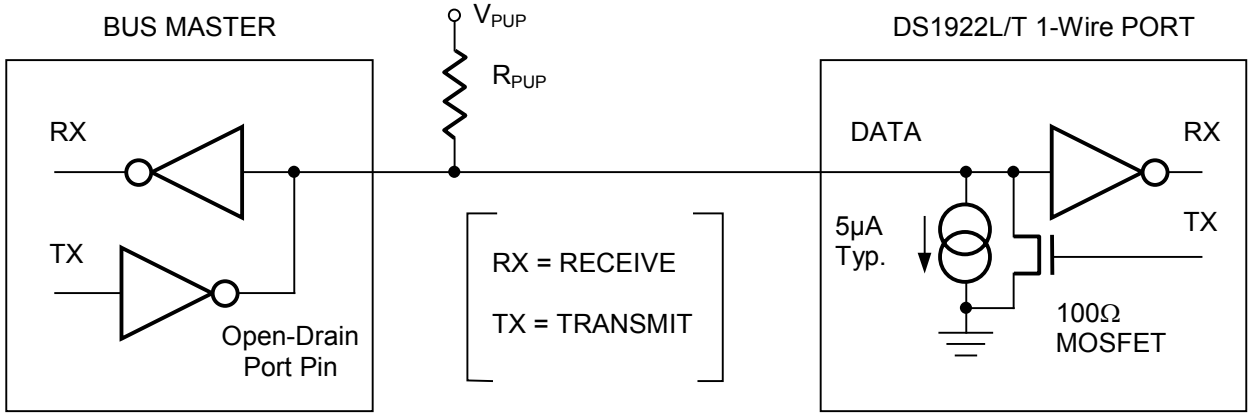
HARDWARE CONFIGURATION

The 1-Wire bus has only a single line by definition; it is important that each device on the bus be able to drive it at the appropriate time. To facilitate this, each device attached to the 1-Wire bus must have open drain or tri-state outputs. The 1-Wire port of the DS1922L/T is open-drain with an internal circuit equivalent to that shown in Figure 10.

A multidrop bus consists of a 1-Wire bus with multiple slaves attached. At standard speed the 1-Wire bus has a maximum data rate of 16.3kbps. The speed can be boosted to 142kbps by activating the Overdrive mode. The DS1922L/T is not guaranteed to be fully compliant to the iButton standard. Its maximum data rate in standard speed mode is 15.4kbps and 125kbps in Overdrive. The value of the pullup resistor primarily depends on the network size and load conditions. The DS1922L/T requires a pullup resistor of maximum 2.2kΩ at any speed.

The idle state for the 1-Wire bus is high. If for any reason a transaction needs to be suspended, the bus MUST be left in the idle state if the transaction is to resume. If this does not occur and the bus is left low for more than 16µs (Overdrive speed) or more than 120µs (standard speed), one or more devices on the bus may be reset. Note that the DS1922L/T does not quite meet the full 16µs maximum low time of the normal 1-Wire bus Overdrive timing. With the DS1922L/T the bus must be left low for no longer than 12µs at Overdrive to ensure that no DS1922L/T on the 1-Wire bus performs a reset. The DS1922L/T communicates properly when used in conjunction with a DS2480B or DS2490 1-Wire driver and adapters that are based on these driver chips.

Figure 10. Hardware Configuration



TRANSACTION SEQUENCE

The protocol for accessing the DS1922L/T through the 1-Wire port is as follows:

- Initialization
- ROM Function Command
- Memory/Control Function Command
- Transaction/Data

INITIALIZATION

All transactions on the 1-Wire bus begin with an initialization sequence. The initialization sequence consists of a reset pulse transmitted by the bus master followed by presence pulse(s) transmitted by the slave(s). The presence pulse lets the bus master know that the DS1922L/T is on the bus and is ready to operate. For more details, see the *1-Wire Signaling* section.

1-Wire ROM FUNCTION COMMANDS

Once the bus master has detected a presence, it can issue one of the eight ROM function commands that the DS1922L/T supports. All ROM function commands are 8 bits long. A list of these commands follows (refer to flowchart in Figure 11).

READ ROM [33H]

This command allows the bus master to read the DS1922L/T's 8-bit family code, unique 48-bit serial number, and 8-bit CRC. This command can only be used if there is a single slave on the bus. If more than one slave is present on the bus, a data collision occurs when all slaves try to transmit at the same time (open drain produces a wired-AND result). The resultant family code and 48-bit serial number results in a mismatch of the CRC.

MATCH ROM [55H]

The Match ROM command, followed by a 64-bit ROM sequence, allows the bus master to address a specific DS1922L/T on a multidrop bus. Only the DS1922L/T that exactly matches the 64-bit ROM sequence responds to the following memory function command. All other slaves wait for a reset pulse. This command can be used with a single or multiple devices on the bus.

SEARCH ROM [F0H]

When a system is initially brought up, the bus master might not know the number of devices on the 1-Wire bus or their registration numbers. By taking advantage of the wired-AND property of the bus, the master can use a process of elimination to identify the registration numbers of all slave devices. For each bit of the registration number, starting with the least significant bit, the bus master issues a triplet of time slots. On the first slot, each slave device participating in the search outputs the true value of its registration number bit. On the second slot, each slave device participating in the search outputs the complemented value of its registration number bit. On the third slot, the master writes the true value of the bit to be selected. All slave devices that do not match the bit written by the master stop participating in the search. If both of the read bits are zero, the master knows that slave devices exist with both states of the bit. By choosing which state to write, the bus master branches in the romcode tree. After one complete pass, the bus master knows the registration number of a single device. Additional passes identify the registration numbers of the remaining devices. Refer to *App Note 187: 1-Wire Search Algorithm* for a detailed discussion, including an example.

CONDITIONAL SEARCH [ECH]

The Conditional Search ROM command operates similarly to the Search ROM command except that only those devices, which fulfill certain conditions, participates in the search. This function provides an efficient means for the bus master to identify devices on a multidrop system that have to signal an important event. After each pass of the conditional search that successfully determined the 64-bit ROM code for a specific device on the multidrop bus, that particular device can be individually accessed as if a Match ROM had been issued, since all other devices will have dropped out of the search process and will be waiting for a reset pulse.

The DS1922L/T will respond to the conditional search if one of the three alarm flags of the Alarm Status Register (address 0214h) reads 1. The temperature alarm will only occur if enabled (see *Temperature Sensor Alarm*). The BOR alarm is always enabled. The first alarm that occurs will make the device respond to the Conditional Search command.

SKIP ROM [CCH]

This command can save time in a single-drop bus system by allowing the bus master to access the memory functions without providing the 64-bit ROM code. If more than one slave is present on the bus and, for example, a Read command is issued following the Skip ROM command, data collision will occur on the bus as multiple slaves transmit simultaneously (open-drain pulldowns will produce a wired-AND result).

RESUME COMMAND [A5h]

The DS1922L/T needs to be accessed several times before a mission will start. In a multidrop environment this means that the 64-bit ROM code after a Match ROM command has to be repeated for every access. To maximize the data throughput in a multidrop environment, the Resume function was implemented. This function checks the status of the RC bit and, if it is set, directly transfers control to the Memory/Control functions, similar to a Skip ROM command. The only way to set the RC bit is through successfully executing the Match ROM, Search ROM, or Overdrive Match ROM command. Once the RC bit is set, the device can repeatedly be accessed through the Resume Command function. Accessing another device on the bus clears the RC bit, preventing two or more devices from simultaneously responding to the Resume Command function.

OVERDRIVE SKIP ROM [3CH]

On a single-drop bus this command can save time by allowing the bus master to access the memory/control functions without providing the 64-bit ROM code. Unlike the normal Skip ROM command, the Overdrive Skip ROM sets the DS1922L/T in the Overdrive mode (OD = 1). All communication following this command has to occur at Overdrive speed until a reset pulse of minimum 690µs duration resets all devices on the bus to standard speed (OD = 0).

When issued on a multidrop bus this command sets all Overdrive-supporting devices into Overdrive mode. To subsequently address a specific Overdrive-supporting device, a reset pulse at Overdrive speed has to be issued followed by a Match ROM or Search ROM command sequence. This speeds up the time for the search process. If more than one slave supporting Overdrive is present on the bus and the Overdrive Skip ROM command is followed by a Read command, data collision occurs on the bus as multiple slaves transmit simultaneously (open-drain pulldowns produce a wired-AND result).

OVERDRIVE MATCH ROM [69H]

The Overdrive Match ROM command followed by a 64-bit ROM sequence transmitted at Overdrive speed allows the bus master to address a specific DS1922L/T on a multidrop bus and to simultaneously set it in Overdrive mode. Only the DS1922L/T that exactly matches the 64-bit ROM sequence responds to the subsequent memory/control function command. Slaves already in Overdrive mode from a previous Overdrive Skip or successful Overdrive Match command remain in Overdrive mode. All overdrive-capable slaves will return to standard speed at the next reset pulse of minimum 690µs duration. The Overdrive Match ROM command can be used with a single or multiple devices on the bus.

Figure 11-1. ROM Funtions Flow Chart

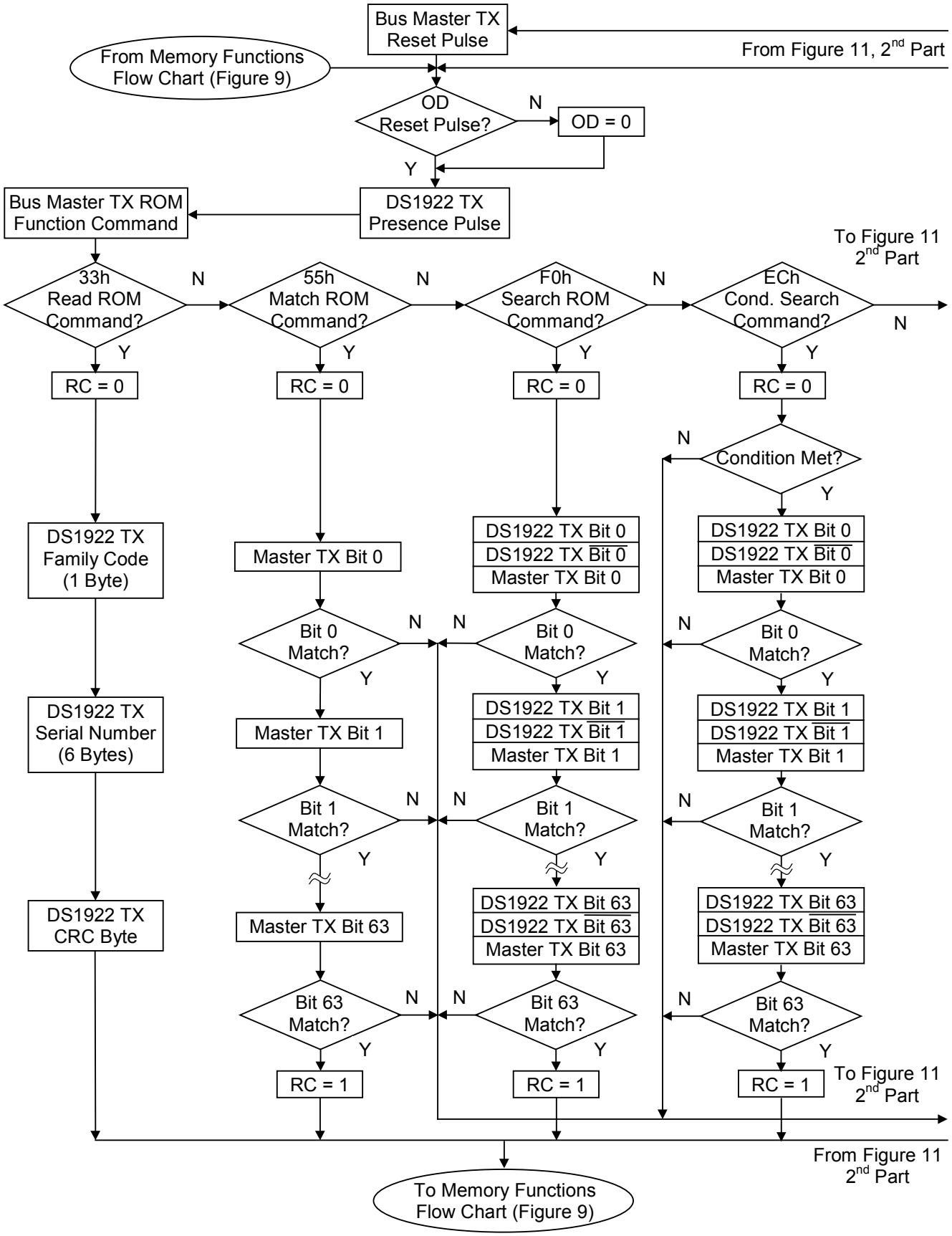
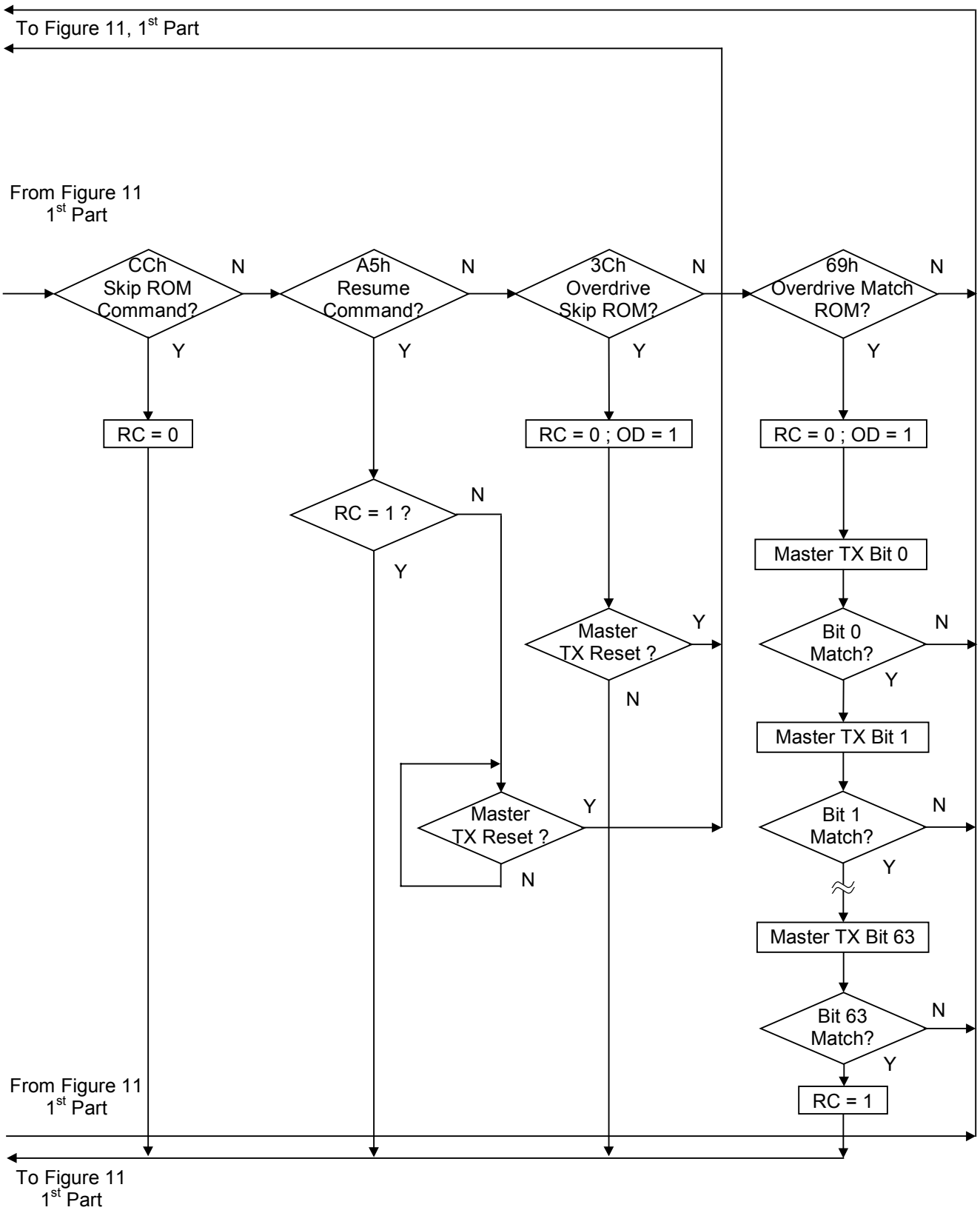


Figure 11-2. ROM Functions Flow Chart



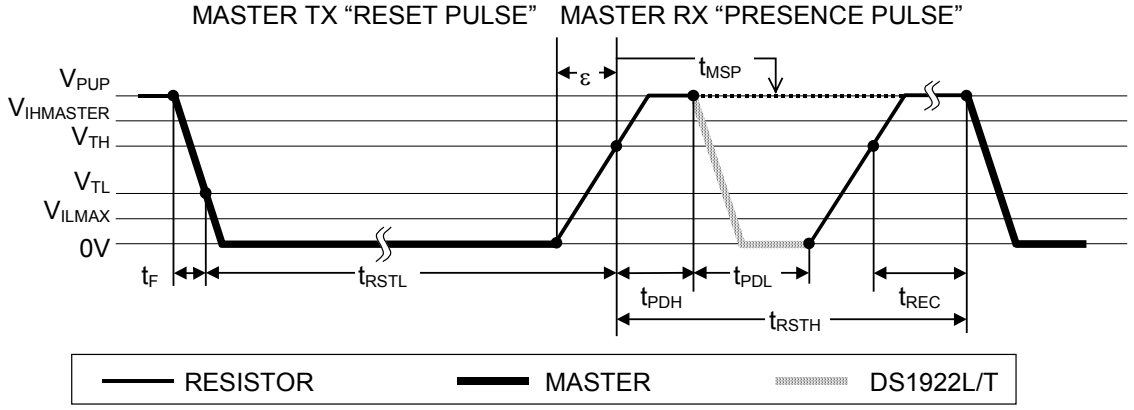
1-Wire SIGNALING

The DS1922L/T requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with reset pulse and presence pulse, write-zero, write-one, and read-data. Except for the presence pulse, the bus master initiates all these signals. The DS1922L/T can communicate at two different speeds, standard speed and Overdrive speed. If not explicitly set into the Overdrive mode, the DS1922L/T will communicate at standard speed. While in Overdrive mode the fast timing applies to all waveforms.

To get from idle to active, the voltage on the 1-Wire line needs to fall from V_{PUP} below the threshold V_{TL}. To get from active to idle, the voltage needs to rise from V_{ILMAX} past the threshold V_{TH}. The time it takes for the voltage to make this rise is seen in Figure 12 as 'ε' and its duration depends on the pullup resistor (R_{PUP}) used and the capacitance of the 1-Wire network attached. The voltage V_{ILMAX} is relevant for the DS1922L/T when determining a logical level, not triggering any events.

The initialization sequence required to begin any communication with the DS1922L/T is shown in Figure 12. A reset pulse followed by a presence pulse indicates the DS1922L/T is ready to receive data, given the correct ROM and memory function command. If the bus master uses slew-rate control on the falling edge, it must pull down the line for $t_{RSTL} + t_F$ to compensate for the edge. A t_{RSTL} duration of 690µs or longer will exit the Overdrive mode returning the device to standard speed. If the DS1922L/T is in Overdrive mode and t_{RSTL} is no longer than 80µs the device will remain in Overdrive mode.

Figure 12. Initialization Procedure "Reset and Presence Pulses"



After the bus master has released the line it goes into receive mode (RX). Now the 1-Wire bus is pulled to V_{PUP} through the pullup resistor or, in case of a DS2480B driver, by active circuitry. When the threshold V_{TH} is crossed, the DS1922L/T waits for t_{PDH} and then transmits a presence pulse by pulling the line low for t_{PDL}. To detect a presence pulse, the master must test the logical state of the 1-Wire line at t_{MSP}.

The t_{RSTH} window must be at least the sum of t_{PDHMAX}, t_{PDLMAX}, and t_{RECMIN}. Immediately after t_{RSTH} is expired, the DS1922L/T is ready for data communication. In a mixed population network t_{RSTH} should be extended to minimum 480µs at standard speed and 48µs at Overdrive speed to accommodate other 1-Wire devices.

READ/WRITE TIME SLOTS

Data communication with the DS1922L/T takes place in time slots, which carry a single bit each. Write time slots transport data from bus master to slave. Read time slots transfer data from slave to master. The definitions of the write and read time slots are illustrated in Figure 13.

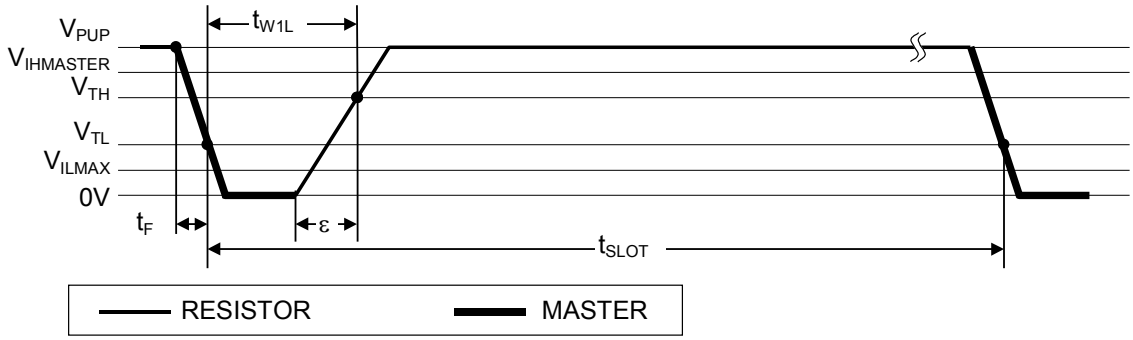
All communication begins with the master pulling the data line low. As the voltage on the 1-Wire line falls below the threshold V_{TL}, the DS1922L/T starts its internal timing generator that determines when the data line is sampled during a write time slot and how long data is valid during a read time slot.

MASTER-TO-SLAVE

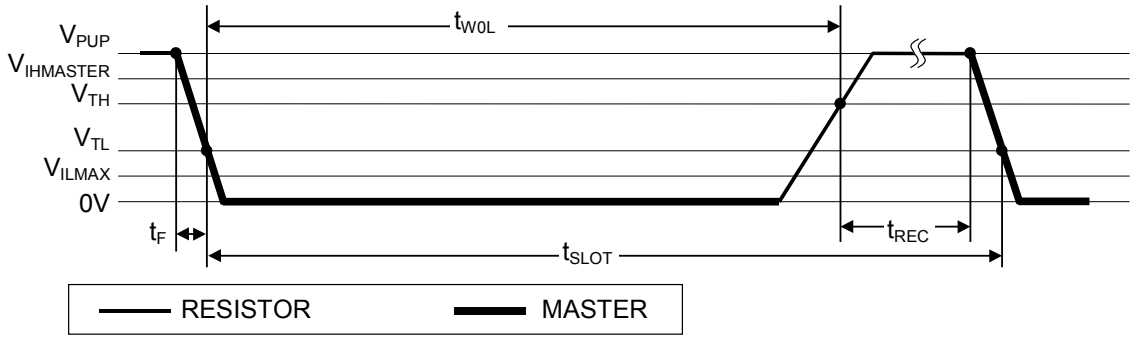
For a **write-one** time slot, the voltage on the data line must have crossed the V_{TH} threshold before the write-one low time t_{W1LMAX} is expired. For a **write-zero** time slot, the voltage on the data line must stay below the V_{TH} threshold until the write-zero low time t_{W0LMIN} is expired. The voltage on the data line should not exceed V_{ILMAX} during the entire t_{W0L} or t_{W1L} window. After the V_{TH} threshold has been crossed, the DS1922L/T needs a recovery time t_{REC} before it is ready for the next time slot.

Figure 13. Read/Write Timing Diagram

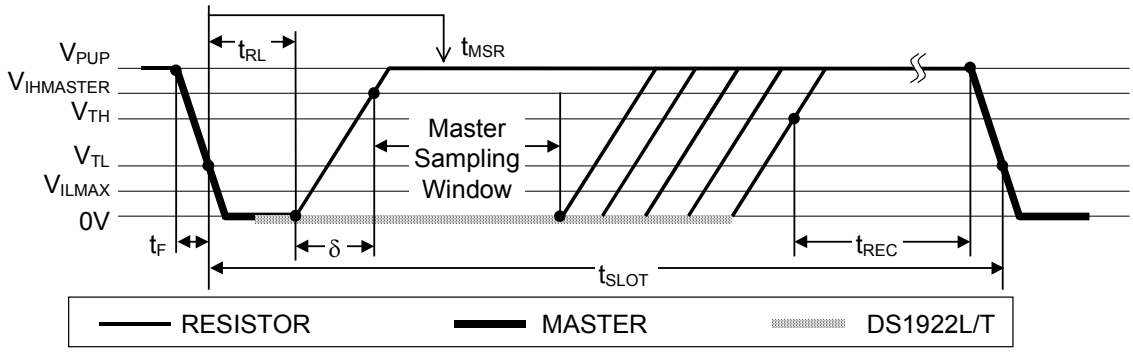
Write-One Time Slot



Write-Zero Time Slot



Read-Data Time Slot



SLAVE-TO-MASTER

A **read-data** time slot begins like a write-one time slot. The voltage on the data line must remain below V_{TL} until the read low time t_{RL} is expired. During the t_{RL} window, when responding with a 0, the DS1922L/T starts pulling the data line low; its internal timing generator determines when this pulldown ends and the voltage starts rising again. When responding with a 1, the DS1922L/T does not hold the data line low at all, and the voltage starts rising as soon as t_{RL} is over.

The sum of t_{RL} + δ (rise rime) on one side and the internal timing generator of the DS1922L/T on the other side define the master sampling window (t_{MSRMIN} to t_{MSRMAX}) in which the master must perform a read from the data line. For most reliable communication, t_{RL} should be as short as permissible and the master should read close to but no later than t_{MSRMAX}. After reading from the data line, the master must wait until t_{SLOT} is expired. This guarantees sufficient recovery time t_{REC} for the DS1922L/T to get ready for the next time slot.

IMPROVED NETWORK BEHAVIOR

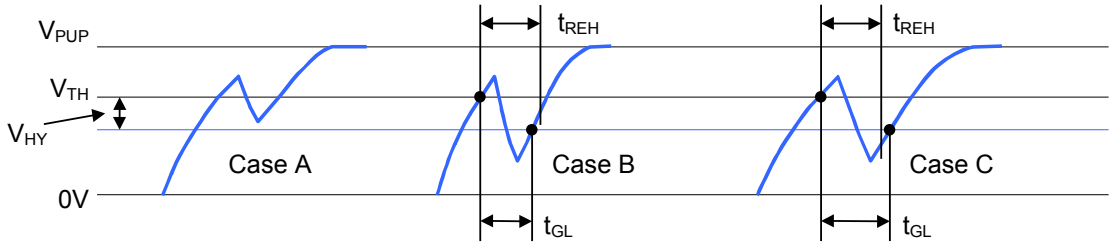
In a 1-Wire environment line termination is possible only during transients controlled by the bus master (1-Wire driver). 1-Wire networks, therefore are susceptible to noise of various origins. Depending on the physical size and topology of the network, reflections from end points, and branch points can add up or cancel each other to some extent. Such reflections are visible as glitches or ringing on the 1-Wire communication line. Noise coupled onto the 1-Wire line from external sources can also result in signal glitching. A glitch during the rising edge of a time slot can cause a slave device to lose synchronization with the master and, as a consequence, result in a search ROM command coming to a dead end or cause a device-specific function command to abort. For better performance in network applications, the DS1922L/T uses a new 1-Wire front end, which makes it less sensitive to noise and also reduces the magnitude of noise injected by the slave device itself.

The 1-Wire front end of the DS1922L/T differs from traditional slave devices in four characteristics:

1) The falling edge of the presence pulse has a controlled slew rate. This provides a better match to the line impedance than a digitally switched transistor, converting the high frequency ringing known from traditional devices into a smoother low-bandwidth transition. The slew rate control is specified by the parameter t_{FPD}, which has different values for standard and Overdrive speed.
2) There is additional low-pass filtering in the circuit that detects the falling edge at the beginning of a time slot. This reduces the sensitivity to high-frequency noise. This additional filtering does not apply at Overdrive speed.
3) There is a hysteresis at the low-to-high switching threshold V_{TH}. If a negative glitch crosses V_{TH} but doesn't go below V_{TH} - V_{HY}, it will not be recognized (Figure 14, Case A). The hysteresis is effective at any 1-Wire speed.
4) There is a time window specified by the rising edge hold-off time t_{REH} during which glitches will be ignored, even if they extend below V_{TH} - V_{HY} threshold (Figure 14, Case B, $t_{GL} < t_{REH}$). Deep voltage droops or glitches that appear late after crossing the V_{TH} threshold and extend beyond the t_{REH} window cannot be filtered out and will be taken as beginning of a new time slot (Figure 14, Case C, $t_{GL} \geq t_{REH}$).

Only devices which have the parameters t_{FPD}, V_{HY} and t_{REH} specified in their electrical characteristics use the improved 1-Wire front end.

Figure 14. Noise Suppression Scheme



CRC GENERATION

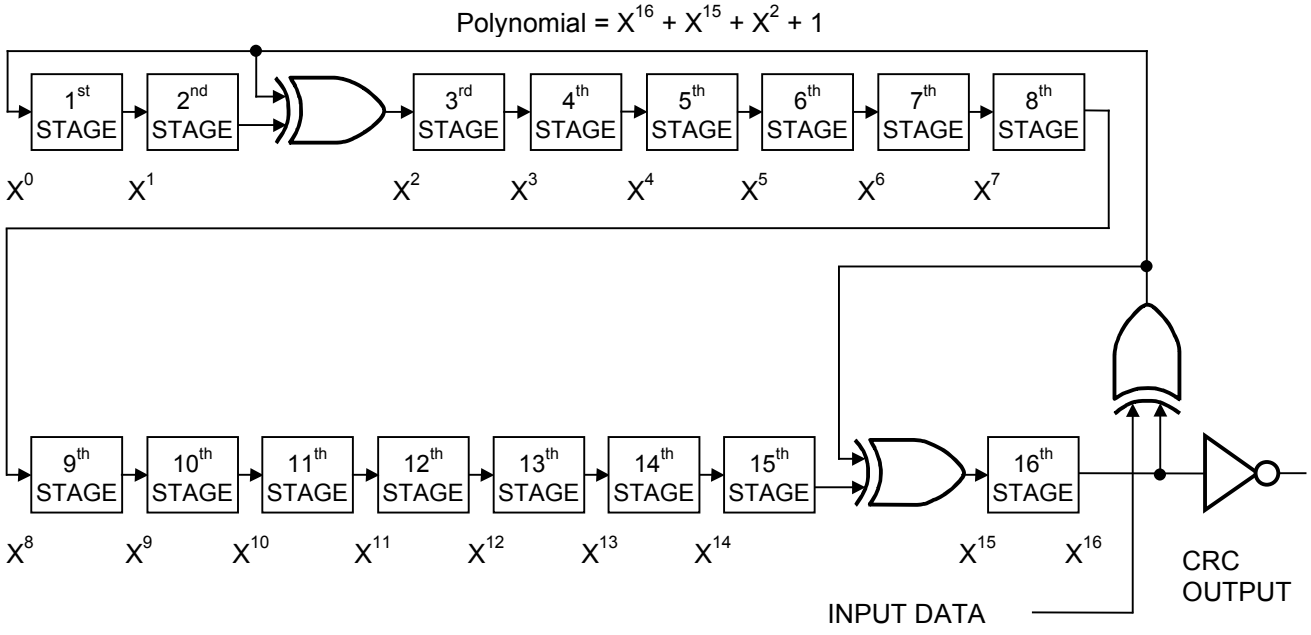
With the DS1922L/T there are two different types of CRCs (Cyclic Redundancy Checks). One CRC is an 8-bit type and is stored in the most significant byte of the 64-bit ROM. The bus master can compute a CRC value from the first 56 bits of the 64-bit ROM and compare it to the value stored within the DS1922L/T to determine if the ROM data has been received error-free. The equivalent polynomial function of this CRC is: $X^8 + X^5 + X^4 + 1$. This 8-bit CRC is received in the true (non-inverted) form. It is computed at the factory and lasered into the ROM.

The other CRC is a 16-bit type, generated according to the standardized CRC16-polynomial function $x^{16} + x^{15} + x^2 + 1$. This CRC is used for error detection when reading register pages or the datalog memory using the Read Memory with CRC command and for fast verification of a data transfer when writing to or reading from the scratchpad. In contrast to the 8-bit CRC, the 16-bit CRC is always communicated in the inverted form. A CRC-generator inside the DS1922L/T (Figure 15) calculates a new 16-bit CRC as shown in the command flow chart of Figure 9. The bus master compares the CRC value read from the device to the one it calculates from the data and decides whether to continue with an operation or to reread the portion of the data with the CRC error. With the initial pass through the Read Memory with CRC flow chart, the 16-bit CRC value is the result of shifting the command byte into the cleared CRC generator, followed by the 2 address bytes and the data bytes. The password is excluded from the CRC calculation. Subsequent passes through the Read Memory with CRC flow chart generate a 16-bit CRC that is the result of clearing the CRC generator and then shifting in the data bytes.

With the Write Scratchpad command the CRC is generated by first clearing the CRC generator and then shifting in the command code, the Target Addresses TA1 and TA2 and all the data bytes. The DS1922L/T transmits this CRC only if the data bytes written to the scratchpad include scratchpad ending offset 11111b. The data may start at any location within the scratchpad.

With the Read Scratchpad command the CRC is generated by first clearing the CRC generator and then shifting in the command code, the Target Addresses TA1 and TA2, the E/S byte, and the scratchpad data starting at the target address. The DS1922L/T transmits this CRC only if the reading continues through the end of the scratchpad, regardless of the actual ending offset. For more information on generating CRC values see *Application Note 27*.

Figure 15. CRC-16 Hardware Description and Polynomial



COMMAND-SPECIFIC 1-Wire COMMUNICATION PROTOCOL—LEGEND

SYMBOL	DESCRIPTION
RST	1-Wire reset pulse generated by master
PD	1-Wire presence pulse generated by slave
Select	Command and data to satisfy the ROM function protocol
WS	Command "Write Scratchpad"
RS	Command "Read Scratchpad"
CPS	Command "Copy Scratchpad with Password"
RMC	Command "Read Memory with Password & CRC"
CM	Command "Clear Memory with Password "
FC	Command "Forced Conversion"
SM	Command "Start Mission with Password"
STP	Command "Stop Mission with Password"
TA	Target Address TA1, TA2
TA-E/S	Target Address TA1, TA2 with E/S byte
<data to EOS>	Transfer of as many data bytes as are needed to reach the scratchpad offset 1Fh
<data to EOP>	Transfer of as many data bytes as are needed to reach the end of a memory page
<data to EOM>	Transfer of as many data bytes as are needed to reach the end of the datalog memory
<PW/dummy>	Transfer of 8 bytes that either represent a valid password or acceptable dummy data
<32 bytes>	Transfer of 32 bytes
<data>	Transfer of an undetermined amount of data
FFh	Transmission of one byte FFh
CRC16\	Transfer of an inverted CRC16
FF loop	Indefinite loop where the master reads FF bytes
AA loop	Indefinite loop where the master reads AA bytes

COMMAND-SPECIFIC 1-Wire COMMUNICATION PROTOCOL—COLOR CODES

Master to slave	Slave to master

WRITE SCRATCHPAD, REACHING THE END OF THE SCRATCHPAD (CANNOT FAIL)

RST	PD	Select	WS	TA	<data to EOS>	CRC16\	FF loop

READ SCRATCHPAD (CANNOT FAIL)

RST	PD	Select	RS	TA-E/S	<data to EOS>	CRC16\	FF loop

COPY SCRATCHPAD WITH PASSWORD (SUCCESS)

RST	PD	Select	CPS	TA-E/S	<PW/dummy>	AA loop

COPY SCRATCHPAD WITH PASSWORD (FAIL TA-E/S OR PASSWORD)

RST	PD	Select	CPS	TA-E/S	<PW/dummy>	FF loop

READ MEMORY WITH PASSWORD AND CRC (SUCCESS)

RST	PD	Select	RMC	TA	<PW/dummy>	<data to EOP>	CRC16\

<32 bytes>	CRC16\	FF loop

Loop

READ MEMORY WITH PASSWORD AND CRC (FAIL PASSWORD OR ADDRESS)

RST	PD	Select	RMC	TA	<PW/dummy>	FF loop

CLEAR MEMORY WITH PASSWORD

RST	PD	Select	CM	<PW/dummy>	FFh	FF loop

To verify success, read the General Status Register at address 0215h. If MEMCLR is 1, the command was executed successfully.

FORCED CONVERSION

RST	PD	Select	FC	FFh	FF loop

To read the result and to verify success, read the addresses 020Ch to 020Fh (results) and the Device Samples Counter at address 0223h to 0225h. If the count has incremented, the command was executed successfully.

START MISSION WITH PASSWORD

RST	PD	Select	SM	<PW/dummy>	FFh	FF loop

To verify success, read the General Status Register at address 0215h. If MIP is 1 and MEMCLR is 0, the command was executed successfully.

STOP MISSION WITH PASSWORD

RST	PD	Select	STP	<PW/dummy>	FFh	FF loop

To verify success, read the General Status Register at address 0215h. If MIP is 0, the command was executed successfully.

MISSION EXAMPLE: PREPARE AND START A NEW MISSION

Assumption: The previous mission has been ended by using the Stop Mission command. Passwords are not enabled. The device is a DS1922L.

Starting a mission requires three steps:

Step 1: Clear the data of the previous mission
Step 2: Write the setup data to register page 1
Step 3: Start the mission

STEP 1

Clear the previous mission.

With only a single device connected to the bus master, the communication of step 1 looks like this:

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse
TX	CCh	Issue “Skip ROM” command
TX	96h	Issue “Clear Memory” command
TX	<8 FFh bytes>	Send dummy password
TX	FFh	Send dummy byte
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse

STEP 2

During the setup, the device needs to learn the following information:

- Time and Date
- Sample Rate
- Alarm Thresholds
- Alarm Controls (Response to Conditional Search)
- General Mission Parameters (e. g., channels to log and logging format, rollover, start mode)
- Mission Start Delay

The following data will setup the DS1922L for a mission that logs temperature using 8-bit format. Such a mission could last up to 56 days until the 8192-byte datalog memory is full.

ADDRESS	DATA	EXAMPLE VALUES	FUNCTION
0200h	00h	15:30:00 hours	Time
0201h	30h		
0202h	15h		
0203h	01h	1st of April in 2002	Date
0204h	04h		
0205h	02h		
0206h	0Ah	Every 10 minutes (EHSS = 0)	Sample rate
0207h	00h		
0208h	52h	0°C low	Temperature Alarm
0209h	66h	10°C high	Threshold
020Ah	00h	(Don’t care)	(Not applicable with DS1922L/T)
020Bh	FFh		(Not applicable with DS1922L/T)

ADDRESS	DATA	EXAMPLE VALUES	FUNCTION
020Ch	FFh	(Don't care)	Clock through read-only registers
020Dh	FFh		
020Eh	FFh		
020Fh	FFh		
0210h	02h	Enable high alarm	Temperature Alarm Control
0211h	FCh	Disabled	(Not applicable with DS1922L/T)
0212h	01h	On (enabled), EHSS = 0 (low sample rate)	RTC Oscillator Control, sample rate selection
0213h	C1h	Normal start; no rollover; 8-bit temp. log	General Mission Control
0214h	FFh	(Don't care)	Clock through read-only registers
0215h	FFh		
0216h	5Ah	90 minutes	Mission Start Delay
0217h	00h		
0218h	00h		

With only a single device connected to the bus master, the communication of step 2 looks like this:

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse
TX	CCh	Issue "Skip ROM" command
TX	0Fh	Issue "Write Scratchpad" command
TX	00h	TA1, beginning offset = 00h
TX	02h	TA2, address = 0200h
TX	<25 data bytes>	Write 25 bytes of data to scratchpad
TX	<7 FFh bytes>	Write through the end of the scratchpad
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse
TX	CCh	Issue "Skip ROM" command
TX	AAh	Issue "Read Scratchpad" command
RX	00h	Read TA1, beginning offset = 00h
RX	02h	Read TA2, address = 0200h
RX	18h	Read E/S, ending offset = 1Fh, flags = 0h
RX	<32 data bytes>	Read scratchpad data and verify
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse
TX	CCh	Issue "Skip ROM" command
TX	99h	Issue "Copy Scratchpad" command
TX	00h	TA1
TX	02h	TA2 (AUTHORIZATION CODE)
TX	1Fh	E/S
TX	<8 FFh bytes>	Send dummy password
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse

STEP 3

Start the new mission.

With only a single device connected to the bus master, the communication of step 3 looks like this:

MASTER MODE	DATA (LSB FIRST)	COMMENTS
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse
TX	CCh	Issue “Skip ROM” command
TX	CCh	Issue “Start Mission” command
TX	<8 FFh bytes>	Send dummy password
TX	FFh	Send dummy byte
TX	(Reset)	Reset pulse
RX	(Presence)	Presence pulse

If step 3 was successful, the MIP bit in the General Status Register will be 1, the MEMCLR bit will be 0 and the mission start delay will count down.

SOFTWARE CORRECTION ALGORITHM FOR TEMPERATURE

The accuracy of the temperature conversion results (forced conversion as well as temperature logs) can be improved through a correction algorithm. The data needed for this software correction is stored in the calibration memory (memory page 18). It consists of reference temperature (Tr) and conversion result (Tc) for two different temperatures, as shown below. See section *Temperature Conversion* for the binary number format.

ADDRESS	DESIGNATOR	DESCRIPTION
0240h	Tr2H	Cold reference temperature, high-byte
0241h	Tr2L	Cold reference temperature, low-byte
0242h	Tc2H	Conversion result at cold reference temperature, high-byte
0243h	Tc2L	Conversion result at cold reference temperature, low-byte
0244h	Tr3H	Hot reference temperature, high-byte
0245h	Tr3L	Hot reference temperature, low-byte
0246h	Tc3H	Conversion result at hot reference temperature, high-byte
0247h	Tc3L	Conversion result at hot reference temperature, low-byte

The software correction algorithm requires two additional values, which are not stored in the device. These values, Tr1 and Offset, are derived from the Device Configuration Byte.

The correction algorithm consists of two steps, preparation and execution. By means of the family code the preparation step verifies whether the device actually is a DS1922. Then the configuration byte is checked to identify the type of DS1922 (L or T). Next three coefficients A, B, and C are computed. In the execution step the temperature reading as delivered by the DS1922 is first converted from the low/high-byte format (TcL, TcH) to °C (Tc) and then corrected to Tcorr. Once step 1 is performed, the three coefficients can be used repeatedly to correct any temperature reading and temperature log *of the same device*.

STEP 1, PREPARATION

Read the 64-bit ROM to obtain the family code. If family code ≠ 41h then stop (wrong device).
Read the Configuration Byte at address 0226h.
If code = 40h then Tr1 = 60, Offset = 41 (DS1922L)
If code = 60h then Tr1 = 90, Offset = 1 (DS1922T)
For all other codes stop (wrong device)
Tr2 = Tr2H/2 + Tr2L/512 - Offset (convert from binary to °C)
Tr3 = Tr3H/2 + Tr3L/512 - Offset (convert from binary to °C)
Tc2 = Tc2H/2 + Tc2L/512 - Offset (convert from binary to °C)
Tc3 = Tc3H/2 + Tc3L/512 - Offset (convert from binary to °C)
Err2 = Tc2 - Tr2
Err3 = Tc3 - Tr3
Err1 = Err2
$B = (Tr2^2 - Tr1^2) * (Err3 - Err1)/[(Tr2^2 - Tr1^2) * (Tr3 - Tr1) + (Tr3^2 - Tr1^2) * (Tr1 - Tr2)]$
$A = B * (Tr1 – Tr2) / (Tr2^2 - Tr1^2)$
$C = Err1 - A * Tr1^2 - B * Tr1$

STEP 2, EXECUTION

Tc = TcH/2 + TcL/512 - Offset (convert from binary to °C)
$Tcorr = Tc - (A * Tc^2 + B * Tc + C)$ (the actual correction)

NOTE: The software correction requires floating point arithmetic (24-bit or better). Suitable math libraries for microcontrollers are found on various websites and are included in cross-compilers.